PolarFire SoC MSS DDR トレーニング状況の確認方法

Fabric 側の DDR は Libero SoC の SmartDebug にて確認するのに対し、 MSS DDR は Memory Log Analyzer を別途インストールして確認します。 Memory Log Analyzer は、2025 年 1 月時点では LPDDR4 と DDR4 のログ確認に 対応しています。 ※ UART が有効となっていることを前提とします。

流れ:

- (1) SoftConsole にてベアメタルのアプリケーション(mpfs-hal-ddr-demo)を実行する
- (2) UART で出力された Terminal 上のログを取り、テキストファイルとして保存する
- (3) Memory Log Analyzer にファイルを読み込ませ、結果を確認
- (4) Memory Log Analyzer の Help から結果に応じた Workaround を確認する



[手順]

 PolarFire SoC のページ > Power Estimators/DDR Memory Analyzer タブより Memory Log Analyzer GUI Installer を入手、インストールします。

https://www.microchip.com/en-us/products/fpgas-and-plds/system-on-chipfpgas/polarfire-soc-fpgas#Documentation

Documentation				
	Search Documer	ntation		
	Search	٩		
Application Notes Data Sheets Power Estimators/DDR Memory Analyzer	Overviews User Guides Pro	oduct Selector Guide		
Title 🗢	Date 👙			
PolarFire FPGA and PolarFire SoC FPGA Power Estimator User Guide	09 Dec 2019	☆		
PolarFire Family Memory Controller User Guide	03 Oct 2024	☆		
Memory Log Analyzer GUI Installer	04 Aug 2023	☆		
PolarFire , PolarFire SoC and RT PolarFire FPGA Power Estimator	24 Oct 2024	☆		

- ② GitHub より bare-metal-example をダウンロードします。
 https://github.com/polarfire-soc/polarfire-soc-bare-metal-examples
- ③ GitHub よりダウンロードした bare-metal-example のうち、 mpfs-hal-ddr-demo プロジェクトをインポートします。





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Search for nested projects
✓ Copy projects into workspace
Close newly imported projects upon completion
Hide projects that already exist in the workspace
Working sets
Add project to working sets New
Working sets: Vortex Select
< Back Next > Einish Cancel



(4) mss_sw_config.h \mathcal{O}

161 行目にて#define DDR_BASE_BOARD のコメントアウトを解除します。



(5) mss_sw_config.h O

#define DEBUG_DDR_INIT と#define DEBUG_DDR_RD_RW_FAIL を

確認します。もしコメントアウトされていたら解除します。

```
199 * See the weak function setup_ddr_
200 * If you need to edit this functic
201 * weak declaration in your applica
202 * */
203 #define DEBUG_DDR_INIT
204 #define DEBUG_DDR_RD_RW_FAIL
205<sup>©</sup> //#define DEBUG_DDR_RD_RW_PASS
206 //#define DEBUG_DDR_CFG_DDR_SGMII_P
207 //#define DEBUG_DDR_DDRCFG
```

- ⑥ 必要に応じて baremetal example にデフォルトで入っている MSS の 構成ファイル(xml ファイル)を差し替えます。
 2 回目のビルドなど、既に xml から生成された fpga_design_config フォルダが ある場合は ビルド前に中身を削除します。
- ⑦ Buid Configurations が妥当かどうか(違い開発キットが選択されていないか等)

	Build Configurations	>	Set Active	>	1 Aries-m100pfsevp-LIM-Debug (DDR4 on Aries M100PFS SOM. Deb			
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**	Run C/C++ Code Analysis	+ + Code Analysis		10 Icicle-Kit-eNVM-Scratchpad-Release (LPDDR4 on Icicle kit. eNVM				



ご確認ください

- ⑧ mpfs-hal-ddr-demo プロジェクトをビルドします。
- ⑨ ボードの電源を入れます。(もし既にデバッガからソフトウェアを走らせている 場合、一度電源を落として再投入して下さい。)
- ⑩ デバッグを実行します。
- Terminal を立ち上げます。
- 12 デバッガを Run します。



 Terminal に表示されたログをテキストファイルにコピー&ペーストし、 保存します。

Start training. TIP CFG PARAMS:07CFE02F dpc bits: 00050422 CFG DDR SGMII PHY->rpc156.rpc156 = 00000001 Spare bit value: 0000A000 PCODE = 00000017NCODE = 0000001Caddr cmd value: 00000000 bclk_sclk_offset_value: 0000000 dpc_vrgen_v_value: 00000000 dpc_vrgen_h_value: 00000000 dpc vrgen vs value: 00000000 tip_cfg_params: 07CFE02F bclk phase 00000300 bclk sclk offset value 00000005 ca_indly 00000000 vref 00000005 a5_dly_max:00000000 a5_dly_min:00000080 a5_dly_min_last:00000080 range_a5:FFFFFF80 deltat:00000080 in_window:00000000 vref_answer:00000080 ca indly 00000000 vref 00000006 a5 dly max:00000000 a5 dly min:00000080 a5_dly_min_last:00000080 range_a5:FFFFFF80 deltat:00000080 in_window:00000000 vref_answer:00000080

⑭ 最初にインストールした Memory Log Analyzer GUI を開きます。





15 ログを保存したテキストファイルを選択します。

Memory Log Analyzer GUI	1.4		-	
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	Memory L	og Analy	zer	
PolarFirea SoC	DDR4			
lease select the log file				
	2	1.		_
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16 結果が表示されます。

Memory Log Analyzer GUI v1.4	-	
<u>у</u> Міскоснір М	lemory Log Analyzer	He
PolarFirea SoC ∨	DDR4 Y	
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	Result	
CA Training Pass Write Levelling Pass Read Gate Training Pass Read DQDQS Training Pass Write Calibration Pass Sanity Check Pass	Message X Training Pass OK	



⑪ Training が fail している場合、Help から Workaround を確認可能です。



以上



変更履歴

リビジョン	日付	概要
V1	2024年1月	新規作成

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