

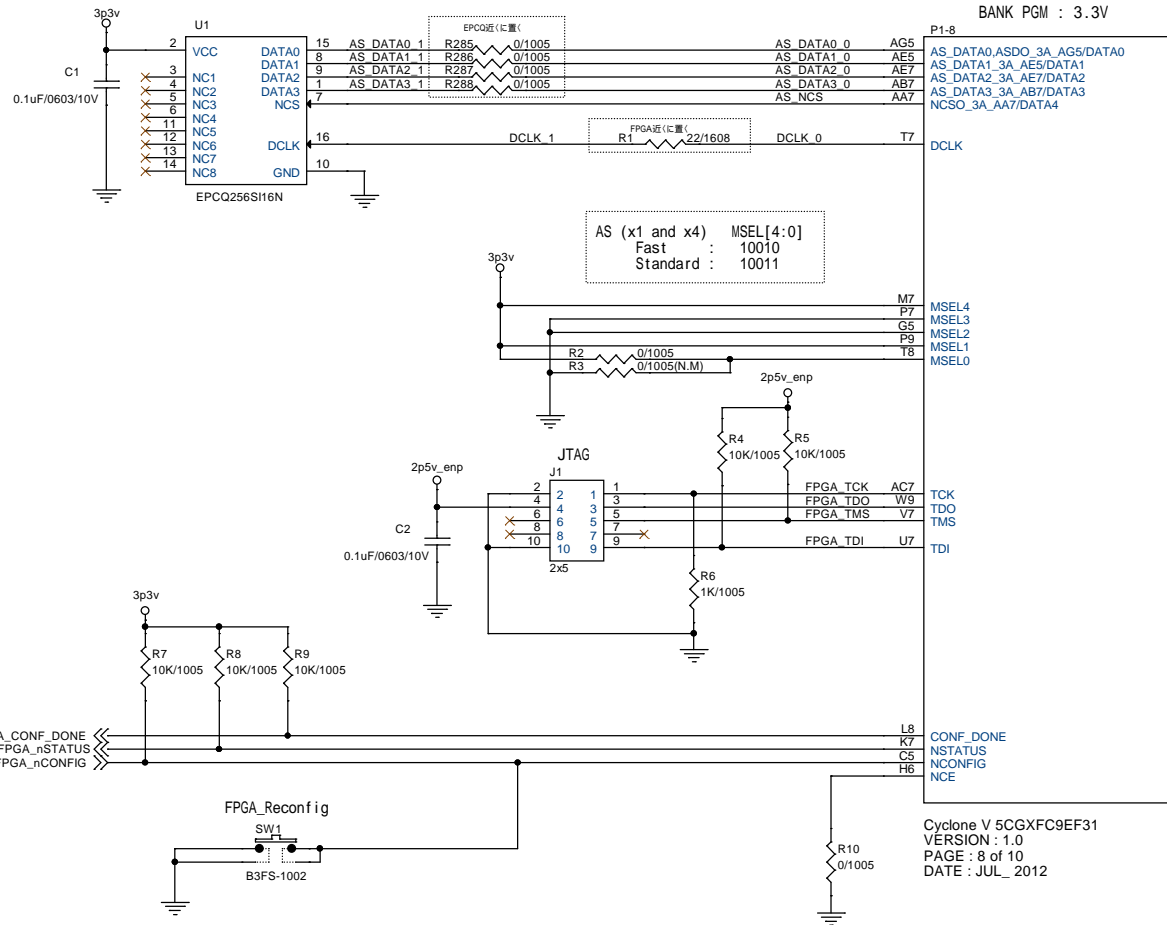
Nitro Schematic

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BANK PGM : 3.3V

AS_DATA0_0	AG5	AS_DATA0_ASDO_3A_AG5/DATA0
AS_DATA1_0	AE5	AS_DATA1_3A_AE5/DATA1
AS_DATA2_0	AE7	AS_DATA2_3A_AE7/DATA2
AS_DATA3_0	AE7	AS_DATA3_3A_AE7/DATA3
AS_NCS	AA7	NCSO_3A_AA7/DATA4
DCLK_0	T7	DCLK
MSEL4	M7	MSEL[4:0]
MSEL3	P7	
MSEL2	G5	
MSEL1	P9	
MSEL0	T8	
TCK	AC7	FPGA_TCK
TDO	W9	FPGA_TDO
TMS	V7	FPGA_TMS
TDI	U7	FPGA_TDI

BANK 3A : 2.5V

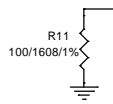
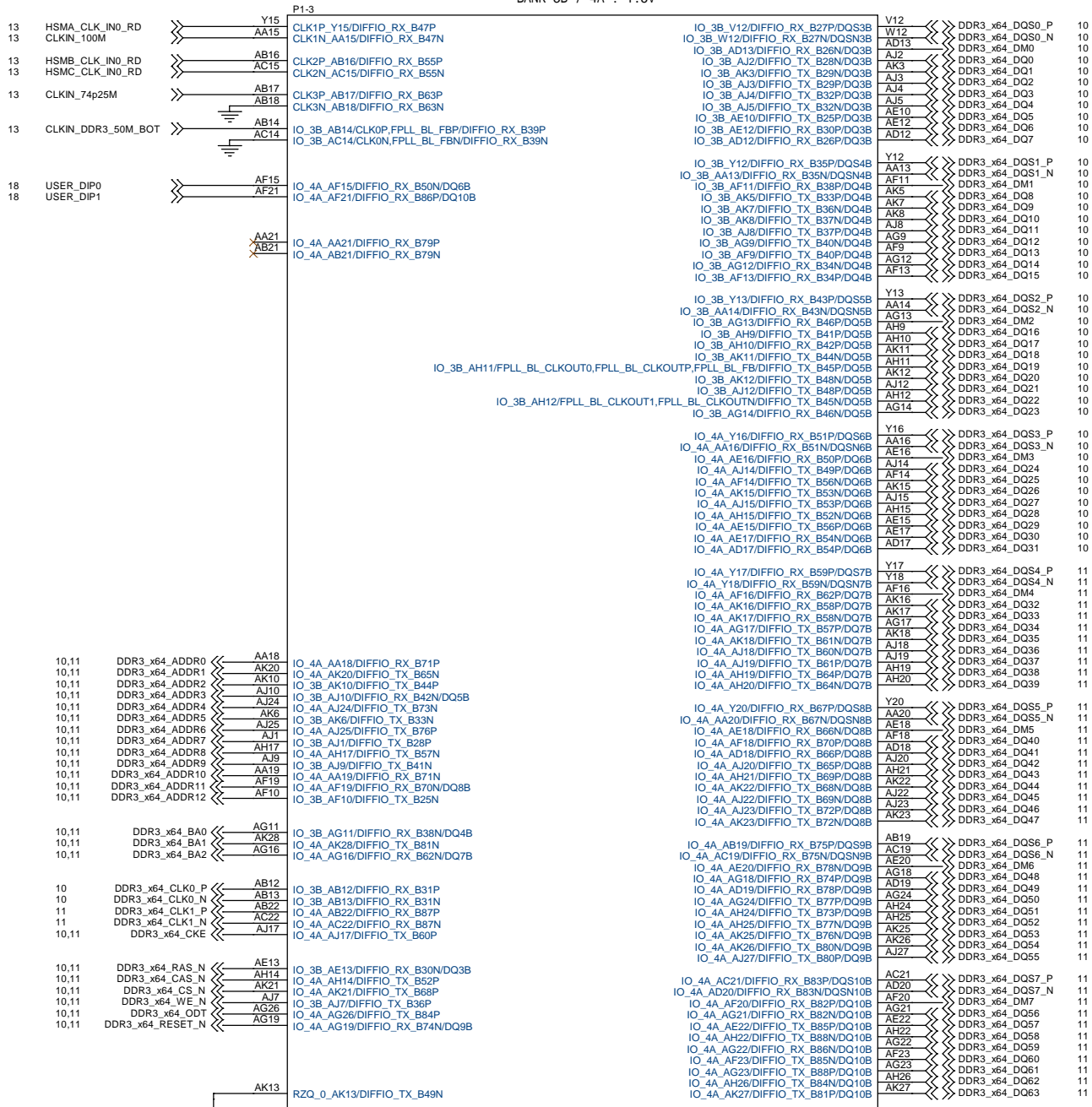
IO_3A_Y10/DATA7/DIFFIO_TX_B2P/DQ1B	Y10	HSMA_CLK_OUT0	15
IO_3A_AA8/DIFFIO_TX_B13P/DQ2B	AA8	HSMA_D0	15
IO_3A_AA9/DIFFIO_TX_B9P/DQ2B	AA9	HSMA_D1	15
IO_3A_AA10/DATA5/DIFFIO_TX_B2N	AA10	HSMA_D3	15
IO_3A_Y11/DATA10/DIFFIO_RX_B3N/DQS1B	Y11	HSMA_SCL	15
IO_3A_AA11/DATA12/DIFFIO_RX_B3P/DQS1B	AA11	HSMA_SDA	15
IO_3A_V9/DATA15/DIFFIO_TX_B6P/DQ1B	V9	HSMB_CLK_OUT0	16
IO_3A_U8/DIFFIO_RX_B11N/DQSN2B	U8	HSMB_D0	16
IO_3A_T9/DIFFIO_RX_B11P/DQS2B	T9	HSMB_D1	16
IO_3A_R10/DATA14/DIFFIO_RX_B5N/DQ1B	R10	HSMB_D3	16
IO_3A_T10/DIFFIO_RX_B15P	T10	HSMB_SCL	16
IO_3A_U9/DIFFIO_RX_B15N	U9	HSMB_SDA	16
IO_3A_AG8/DIFFIO_TX_B12N/DQ2B	AG8	HSMC_D62	17
IO_3A_AF8/DIFFIO_TX_B12P	AF8	HSMC_D63	17
IO_3A_AH7/DIFFIO_TX_B16N/DQ2B	AH7	HSMC_D64	17
IO_3A_AG7/DIFFIO_TX_B16P/DQ2B	AG7	HSMC_D65	17
IO_3A_AF7/DIFFIO_TX_B8P/DQ1B	AF6	HSMC_D66	17
IO_3A_AH6/DIFFIO_RX_B10N/DQ2B	AH6	HSMC_D67	17
IO_3A_AG6/DIFFIO_RX_B10P/DQ2B	AG6	HSMC_D68	17
IO_3A_AF6/PR_READY/DIFFIO_TX_B8N/DQ1B	AF6	HSMC_D69	17
IO_3A_AH5/DIFFIO_RX_B14N/DQ2B	AH5	HSMC_D70	17
IO_3A_AH4/DIFFIO_RX_B14P/DQ2B	AH4	HSMC_D71	17
IO_3A_AD9/DATA9/DIFFIO_TX_B4N/DQ1B	AD9	HSMC_D72	17
IO_3A_AC9/DATA11/DIFFIO_TX_B4P	AC9	HSMC_D73	17
IO_3A_AB9/DIFFIO_TX_B9N	AB9	HSMC_D74	17
IO_3A_AB8/DIFFIO_TX_B13N/DQ2B	AB8	HSMC_D75	17
IO_3A_V11/PR_ERROR/DIFFIO_RX_B7P	V11	USER_LED0_N	18
IO_3A_U11/DATA8/DIFFIO_RX_B1P/DQ1B	U11	USER_LED1_N	18
IO_3A_T11/CLKUSR/DIFFIO_RX_B5P/DQ1B	T11	USER_LED2_N	18
IO_3A_U12/DATA6/DIFFIO_RX_B1N/DQ1B	U12	USER_LED3_N	18
IO_3A_V10/PR_DONE/DIFFIO_RX_B7N	V10	SIS338_SCL	13
IO_3A_W10/DATA13/DIFFIO_TX_B6N/DQ1B	W10	SIS338_SDA	13

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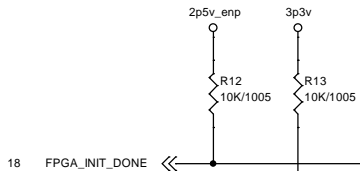
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BANK 3B / 4A : 1.5V



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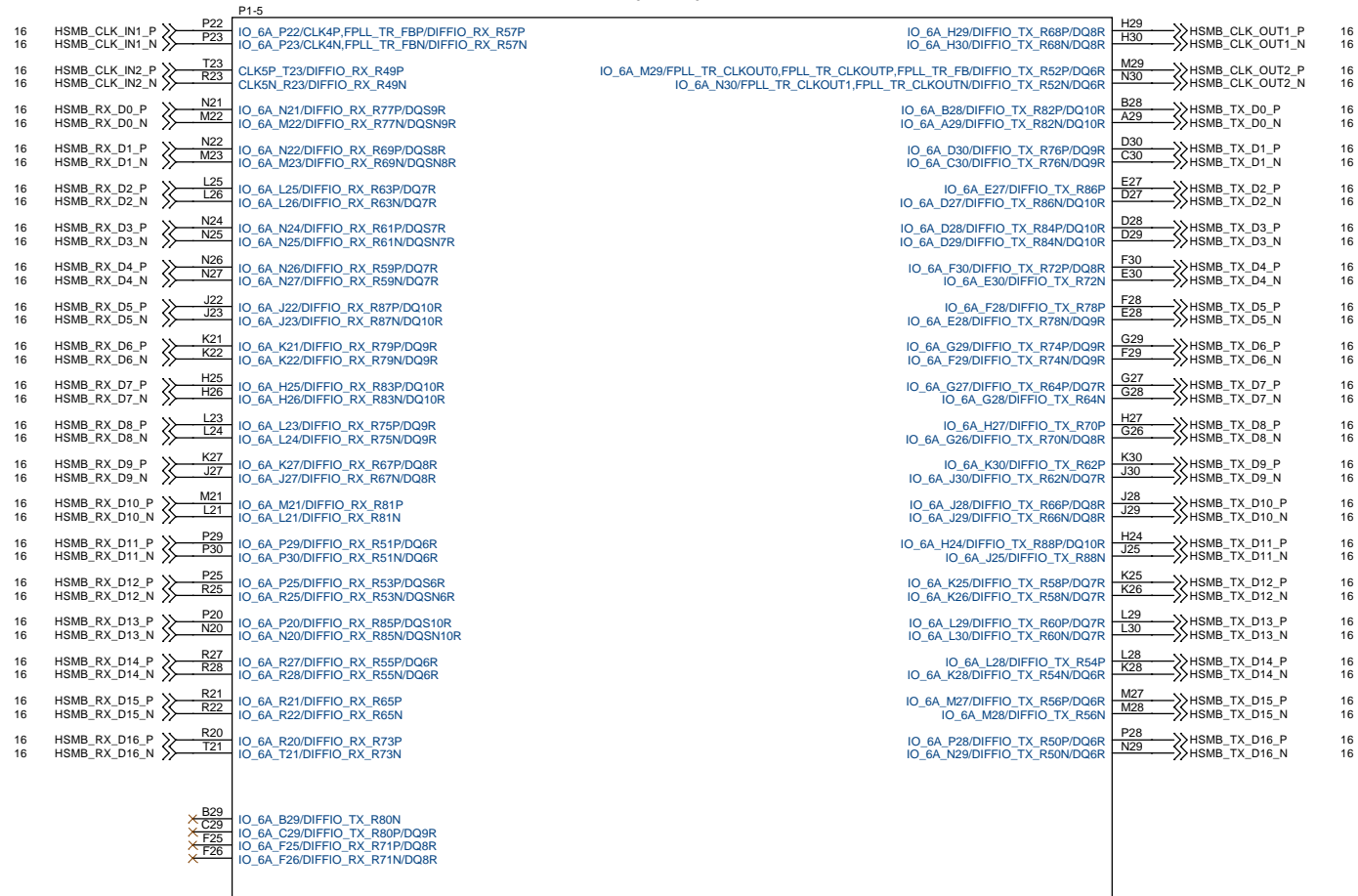
BANK 5A / 5B : 2.5V

18	FPGA_INIT_DONE	W22	IO_5A_W22/INIT_DONE/DIFFIO_RX_R2P	IO_5B_R30/DIFFIO_RX_R47N/DQ5R	R30	HSMC_SDA	17
		AD25	IO_5A_AD25/CVP_CONF/DONE/DIFFIO_TX_R3N/DQ1R	IO_5B_T30/DIFFIO_RX_R47P/DQ5R	T30	HSMC_SCL	17
18	USER_GPIO5	AA26	IO_5A_AA26/DEV_CLRND/DIFFIO_TX_R5N/DQ1R	IO_5B_U29/DIFFIO_TX_R48P/DQ5R	U29	HSMC_CLK_OUT0	17
15	HSM_A_D2	W24	IO_5A_W24/NPERSTL1/DIFFIO_RX_R6N/DQS1R	IO_5B_T29/DIFFIO_RX_R43N/DQ5R	T29	HSMC_D0	17
16	HSM_B_D2	Y23	IO_5A_Y23/NPERSTL0/DIFFIO_RX_R6P/DQS1R	IO_5B_T28/DIFFIO_RX_R43P/DQ5R	T28	HSMC_D1	17
18	USER_GPIO0	V21	IO_5A_V21/DIFFIO_RX_R21P/DQS2R	IO_5B_R26/DIFFIO_RX_R45N/DQS5R	R26	HSMC_D2	17
18	USER_GPIO1	V22	IO_5A_V22/DIFFIO_RX_R21N/DQS2R	IO_5B_T25/DIFFIO_RX_R45P/DQS5R	T25	HSMC_D3	17
18	USER_GPIO2	AE23	IO_5A_AE23/DIFFIO_TX_R18P/DQ2R	IO_5B_U28/DIFFIO_RX_R37N/DQS4R	U28	HSMC_D4	17
18	USER_GPIO3	Y21	IO_5A_Y21/CRC_ERROR/DIFFIO_RX_R2N	IO_5B_U27/DIFFIO_RX_R37P/DQS4R	U27	HSMC_D5	17
18	USER_GPIO4	AF24	IO_5A_AF24/DIFFIO_TX_R18N/DQ2R	IO_5B_U26/DIFFIO_RX_R29N/DQS3R	U26	HSMC_D6	17
		V30	IO_5B_V30/DIFFIO_TX_R48N	IO_5B_V29/DIFFIO_TX_R46P	V29	HSMC_D7	17
			IO_5B_W30/FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTN,DIFFIO_TX_R44N/DQ5R	IO_5B_V27/DIFFIO_RX_R35P/DQ4R	V27	HSMC_D8	17
			IO_5B_W29/DIFFIO_TX_R46N/DQ5R	IO_5B_V26/DIFFIO_RX_R29P/DQS3R	V26	HSMC_D9	17
			IO_5B_W28/DIFFIO_RX_R35N/DQ4R	IO_5B_V25/DIFFIO_RX_R25N	V25	HSMC_D10	17
			IO_5A_W27/DIFFIO_RX_R23N/DQ2R	IO_5B_V24/DIFFIO_RX_R25P	V24	HSMC_D11	17
			IO_5B_Y28/DIFFIO_RX_R27N/DQ3R	IO_5B_W30/FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTN,DIFFIO_TX_R44N/DQ5R	W30	HSMC_D12	17
			IO_5A_Y27/DIFFIO_RX_R23P/DQ2R	IO_5B_W29/DIFFIO_TX_R46N/DQ5R	W29	HSMC_D13	17
			IO_5A_Y26/DIFFIO_RX_R4N/DQ1R	IO_5B_W28/DIFFIO_RX_R35N/DQ4R	W28	HSMC_D14	17
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			IO_5B_AA30/DIFFIO_RX_R39N/DQ4R	IO_5A_Y27/DIFFIO_RX_R23P/DQ2R	Y27	HSMC_D17	17
			IO_5B_AA29/DIFFIO_RX_R39P/DQ4R	IO_5A_Y26/DIFFIO_RX_R4N/DQ1R	Y26	HSMC_D18	17
			IO_5B_AA28/DIFFIO_RX_R27P/DQ3R	IO_5A_Y25/DIFFIO_RX_R4P/DQ1R	Y25	HSMC_D19	17
			IO_5A_AA25/DIFFIO_RX_R17N	IO_5A_Y22/DIFFIO_RX_R8P/DQ1R	Y22	HSMC_D20	17
			IO_5A_AA24/DIFFIO_RX_R17P	IO_5B_AA30/DIFFIO_RX_R39N/DQ4R	AA30	HSMC_D21	17
			IO_5A_AA23/DIFFIO_RX_R9N/DQ1R	IO_5B_AA29/DIFFIO_RX_R39P/DQ4R	AA29	HSMC_D22	17
			IO_5B_AB29/DIFFIO_TX_R42P/DQ5R	IO_5B_AA28/DIFFIO_RX_R27P/DQ3R	AA28	HSMC_D23	17
			IO_5B_AB28/DIFFIO_TX_R40N	IO_5A_AA25/DIFFIO_RX_R17N	AA25	HSMC_D24	17
			IO_5B_AB27/DIFFIO_TX_R40P/DQ4R	IO_5A_AA24/DIFFIO_RX_R17P	AA24	HSMC_D25	17
			IO_5A_AB26/DEV_OE/DIFFIO_TX_R5P	IO_5A_AA23/DIFFIO_RX_R9N/DQ1R	AA23	HSMC_D26	17
			IO_5B_AC30/DIFFIO_TX_R42N/DQ5R	IO_5B_AB29/DIFFIO_TX_R42P/DQ5R	AB29	HSMC_D27	17
			IO_5B_AC29/DIFFIO_TX_R38N/DQ4R	IO_5B_AB28/DIFFIO_TX_R40N	AB28	HSMC_D28	17
			IO_5A_AC27/DIFFIO_TX_R7N	IO_5B_AB27/DIFFIO_TX_R40P/DQ4R	AB27	HSMC_D29	17
			IO_5A_AC26/DIFFIO_TX_R7P/DQ1R	IO_5A_AB26/DEV_OE/DIFFIO_TX_R5P	AB26	HSMC_D30	17
				IO_5B_AC30/DIFFIO_TX_R42N/DQ5R	AC30	HSMC_D31	17
				IO_5B_AC29/DIFFIO_TX_R38N/DQ4R	AC29	HSMC_D32	17
				IO_5A_AC27/DIFFIO_TX_R7N	AC27	HSMC_D33	17
				IO_5A_AC26/DIFFIO_TX_R7P/DQ1R	AC26	HSMC_D34	17
				IO_5B_AE30/DIFFIO_RX_R31P/DQ3R	AE30	HSMC_D35	17
				IO_5B_AD30/DIFFIO_RX_R31N/DQ3R	AD30	HSMC_D36	17
				CLK6P_U23/DIFFIO_RX_R41P	U23	HSMC_D37	17
				CLK6N_T24/DIFFIO_RX_R41N	T24	HSMC_D38	17
				IO_5A_AC24/PR_REQUEST/DIFFIO_TX_R1N/DQ1R	AC24	HSMC_D39	17
				IO_5B_AD29/DIFFIO_TX_R38P	AD29	HSMC_D40	17
				IO_5B_AD28/DIFFIO_TX_R36N/DQ4R	AD28	HSMC_D41	17
				IO_5A_AD27/DIFFIO_RX_R19N/DQ2R	AD27	HSMC_D42	17
				RZQ_1_AD23/DIFFIO_TX_R1P/DQ1R	AD24	HSMC_D43	17
				IO_5B_AE28/DIFFIO_TX_R36P/DQ4R	AD23	HSMC_D44	17
				IO_5A_AE27/DIFFIO_RX_R19P/DQ2R	AE28	HSMC_D45	17
				IO_5A_AE26/DIFFIO_TX_R20N/DQ2R	AE27	HSMC_D46	17
				IO_5A_AE25/DIFFIO_TX_R20P/DQ2R	AE26	HSMC_D47	17
				IO_5B_AF30/DIFFIO_TX_R34N/DQ4R	AE25	HSMC_D48	17
				IO_5B_AF29/DIFFIO_TX_R34P/DQ4R	AF30	HSMC_D49	17
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				IO_5A_AF26/DIFFIO_TX_R22N/DQ2R	AF28	HSMC_D51	17
				IO_5A_AF25/DIFFIO_TX_R22P	AF26	HSMC_D52	17
				IO_5B_AG29/DIFFIO_TX_R28N/DQ3R	AG29	HSMC_D53	17
				IO_5B_AG28/DIFFIO_TX_R32P/DQ3R	AG28	HSMC_D54	17
				IO_5A_AG27/DIFFIO_TX_R24N	AG27	HSMC_D55	17
				IO_5B_AH30/DIFFIO_TX_R30N/DQ3R	AG26	HSMC_D56	17
				IO_5B_AH29/DIFFIO_TX_R28P/DQ3R	AH30	HSMC_D57	17
				IO_5A_AH27/DIFFIO_TX_R24P/DQ2R	AH29	HSMC_D58	17
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				IO_5B_AJ28/DIFFIO_TX_R26P/DQ3R	AJ30	HSMC_D60	17
				IO_5B_AJ29/DIFFIO_TX_R26N/DQ3R	AJ28	HSMC_D61	17
				IO_5B_U21/CLK7P,FPLL_BR_FBP/DIFFIO_RX_R33P	AJ29	HSMC_D76	17
				IO_5B_U22/CLK7N,FPLL_BR_FBN/DIFFIO_RX_R33N	AJ29	HSMC_D78	17
					U21	HSMC_D77	17
					U22	HSMC_D79	17

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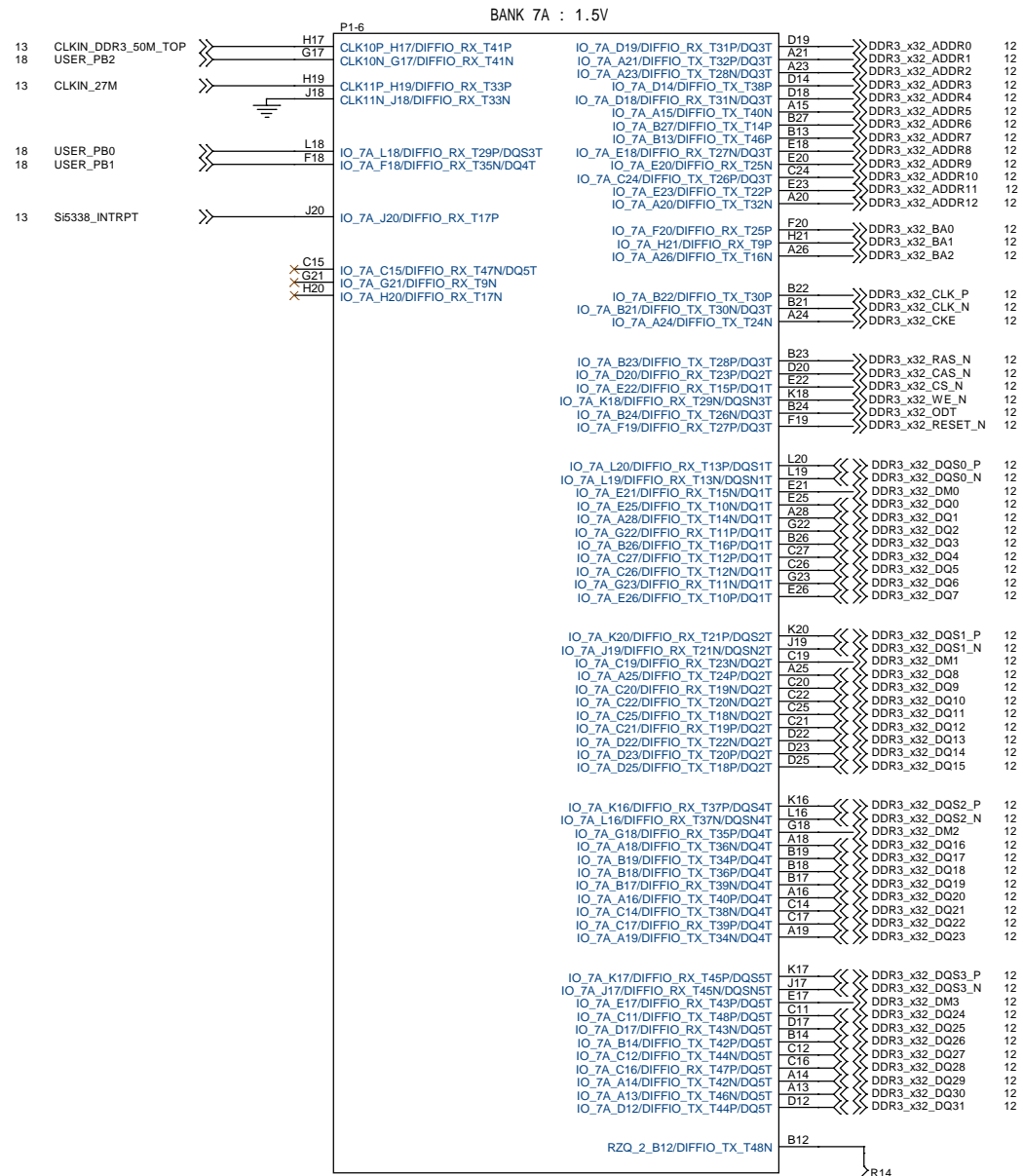
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BANK 6A : 2.5V

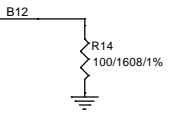


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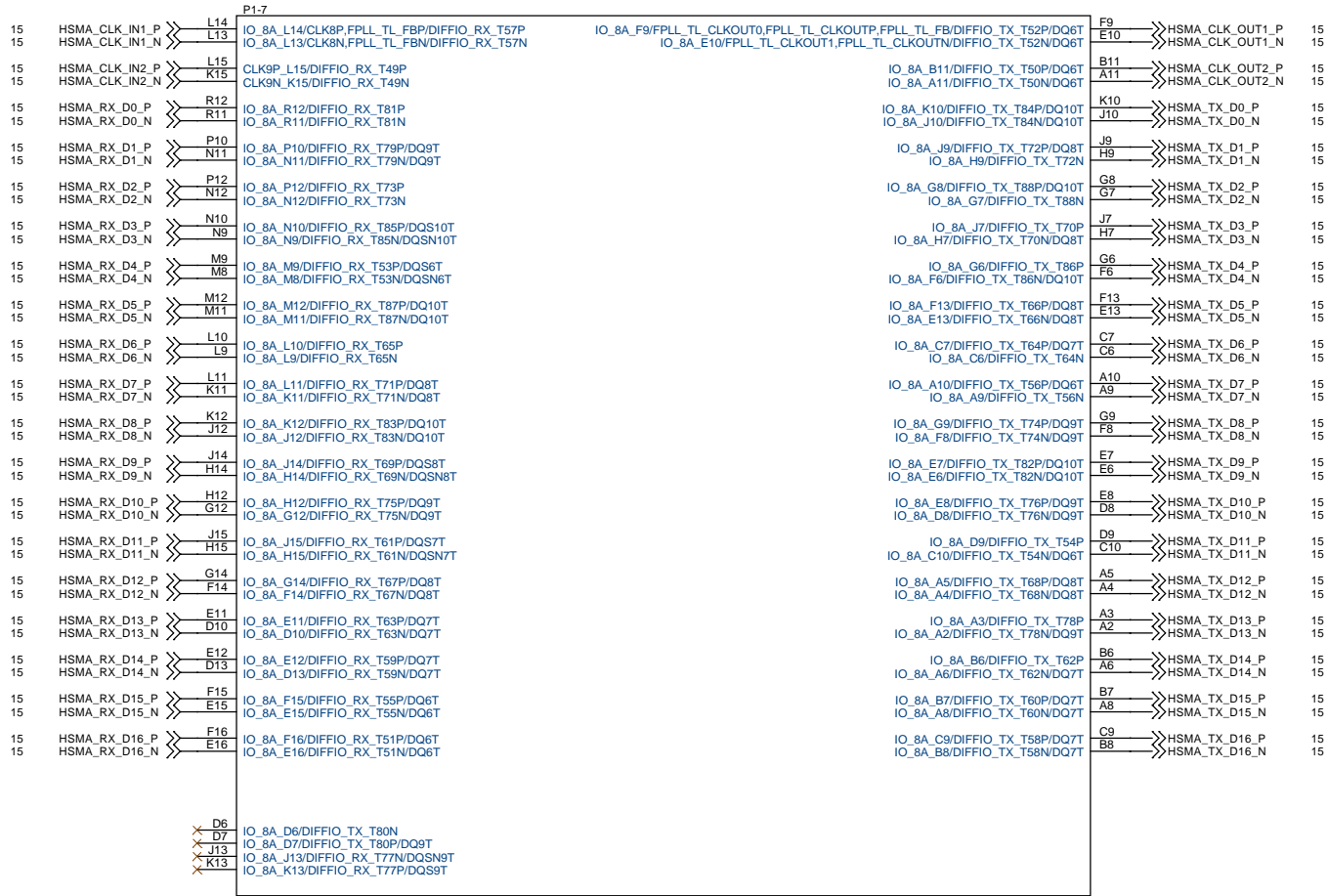


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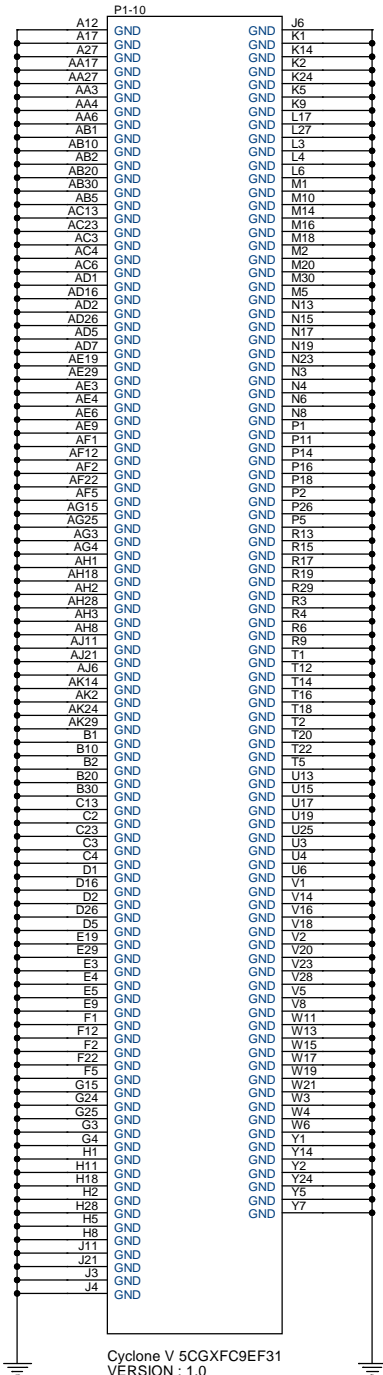
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BANK 8A : 2.5V

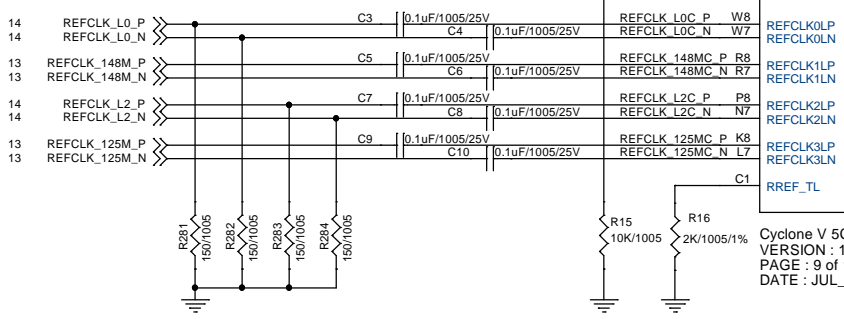
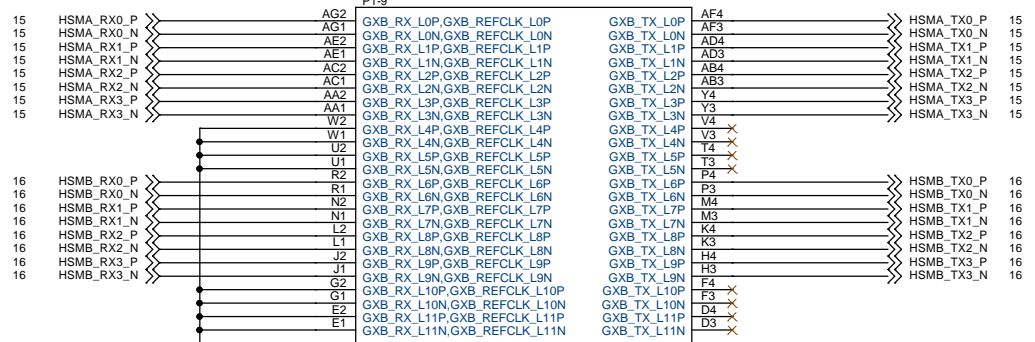


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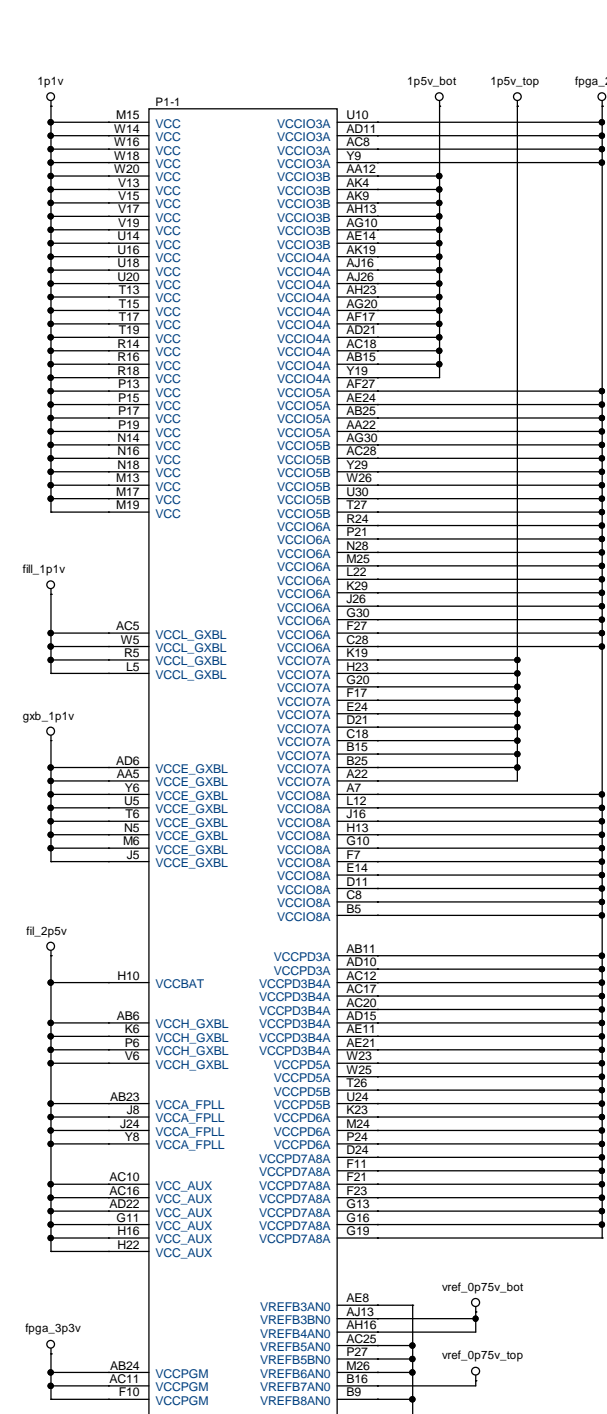


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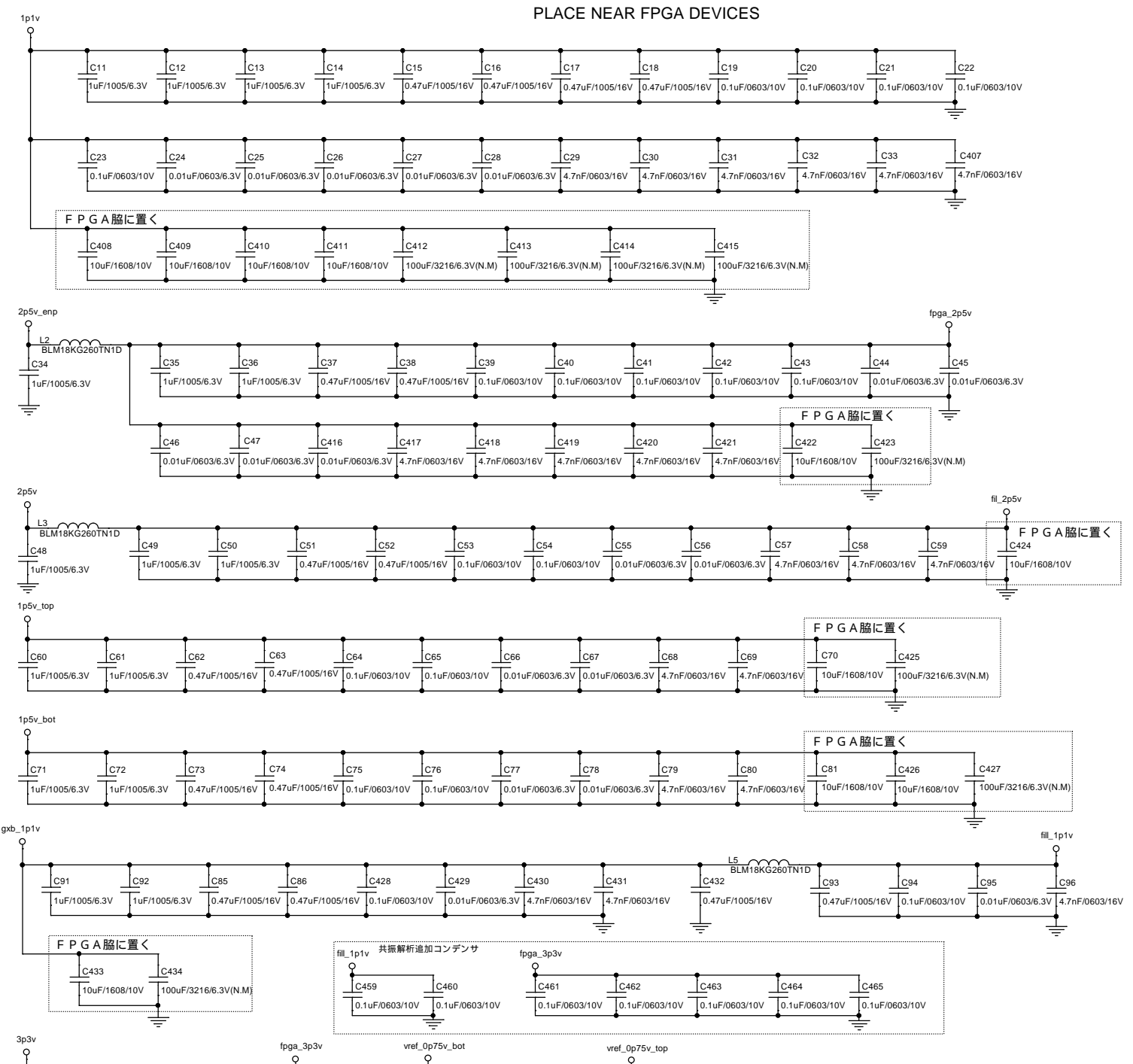


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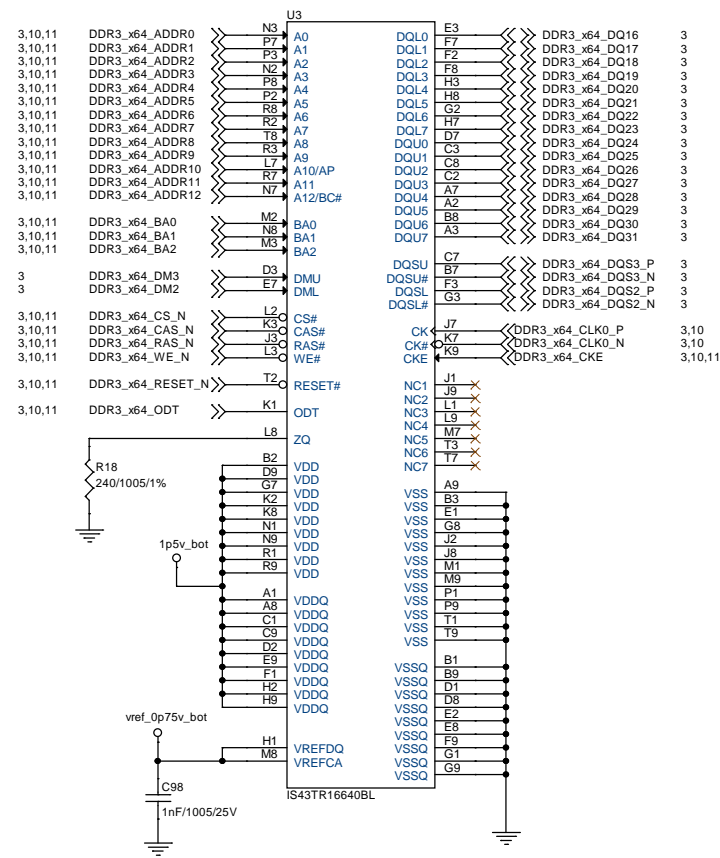
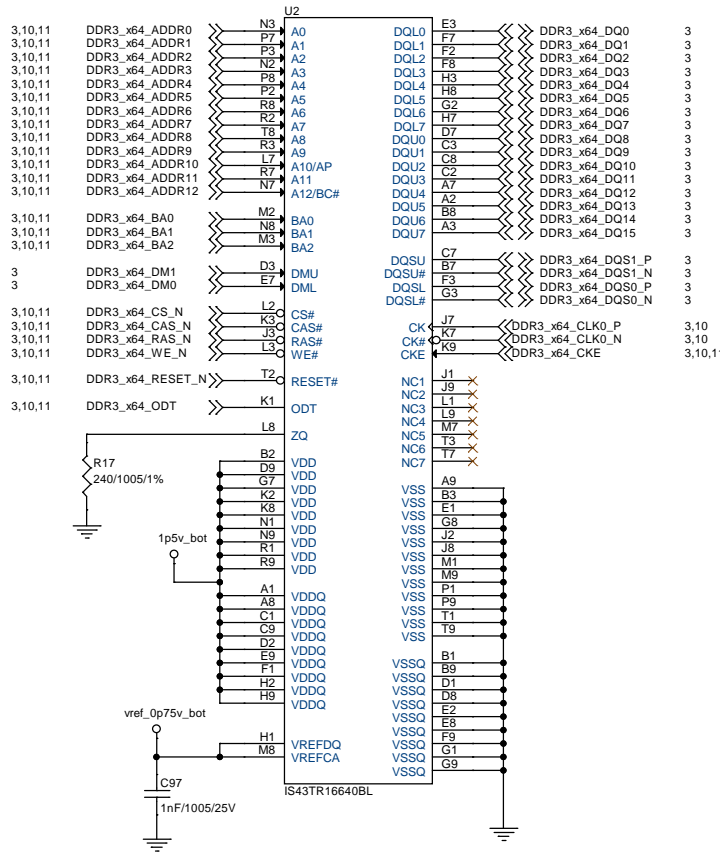


PLACE NEAR FPGA DEVICES

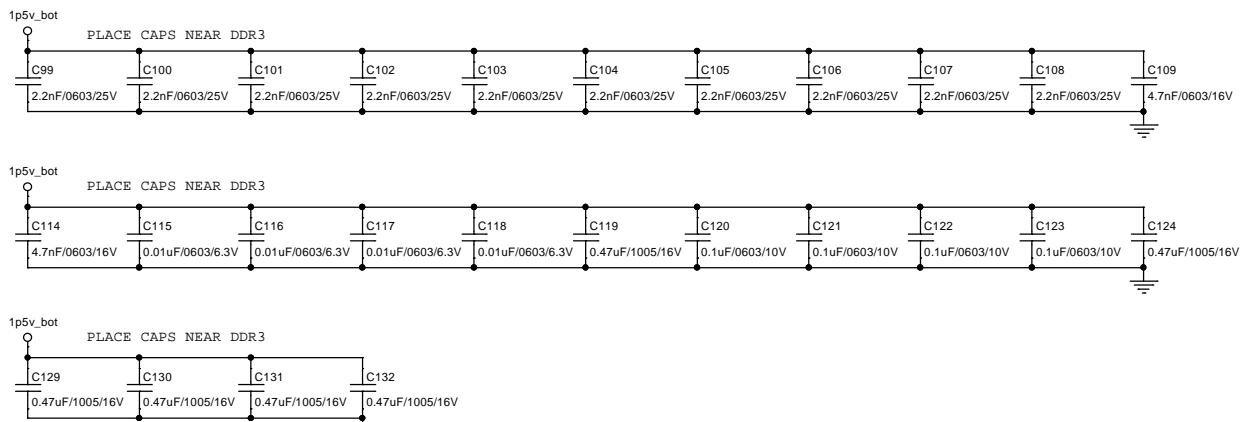
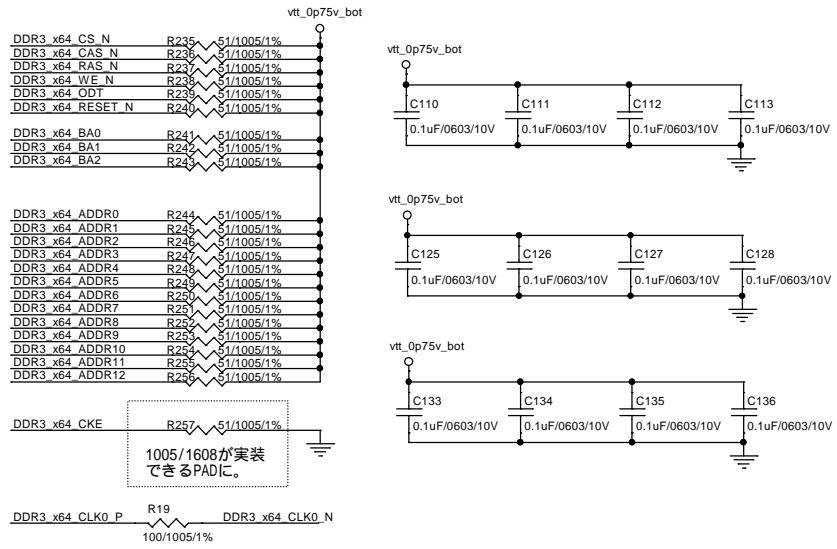


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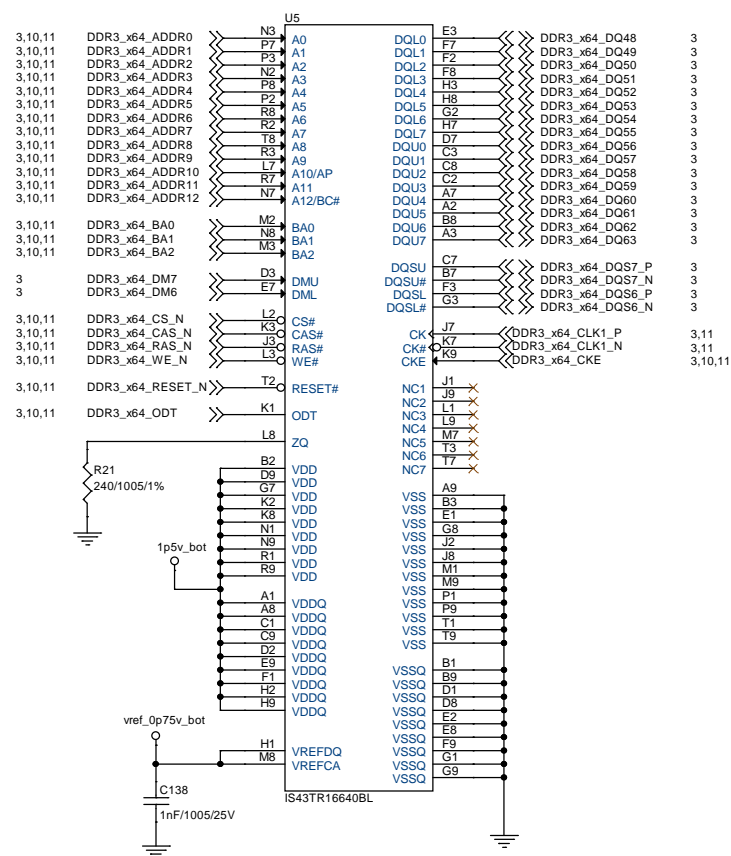
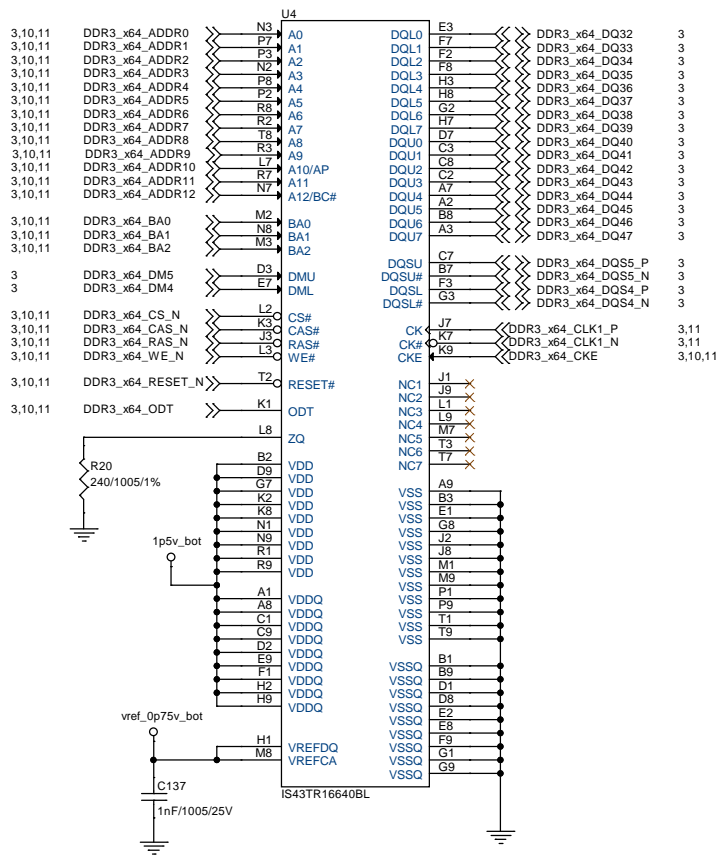
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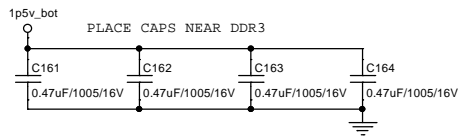
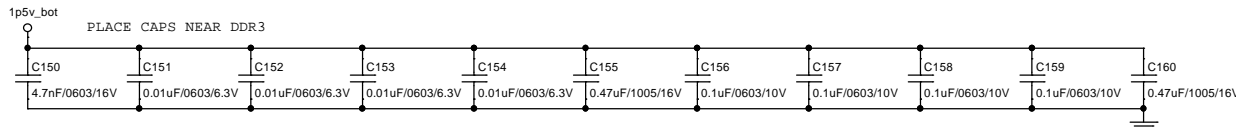
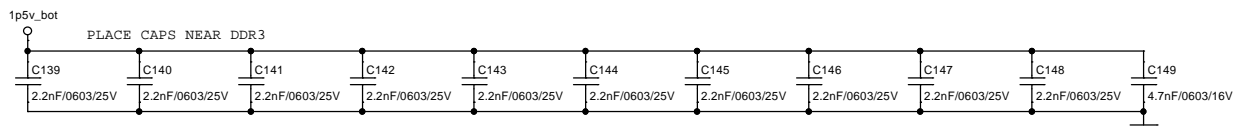


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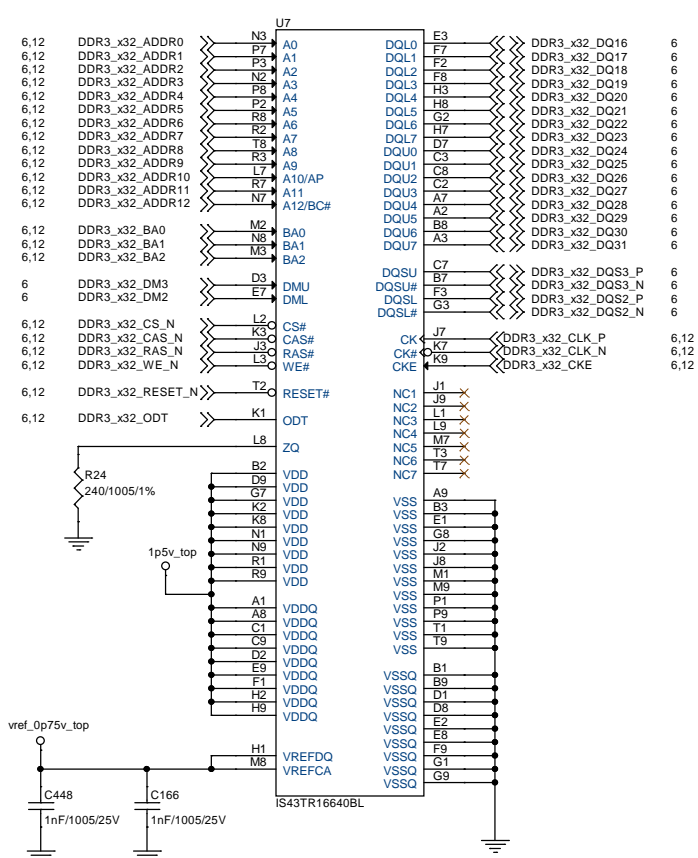
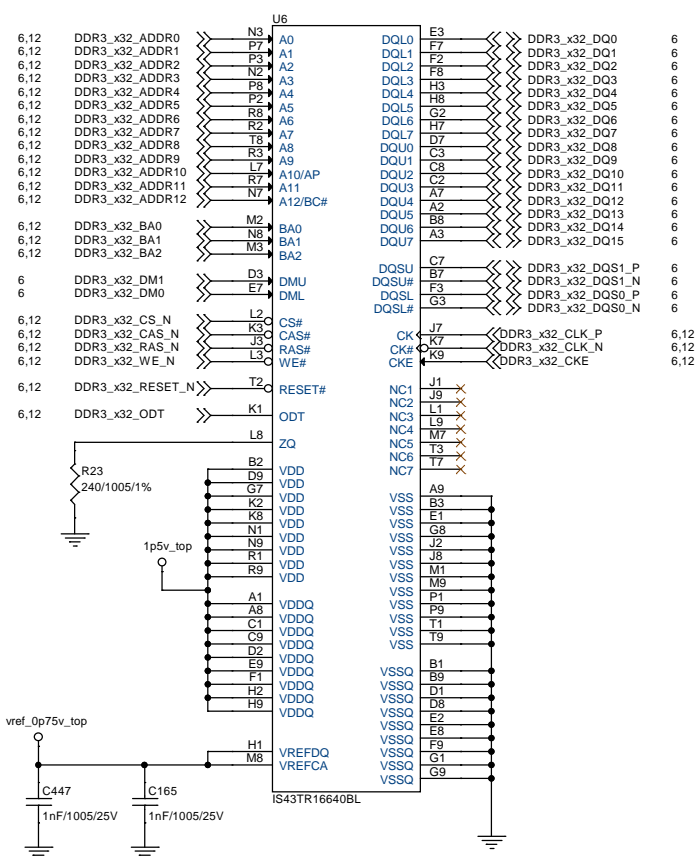


PLACE NEAR DDR3 DEVICES

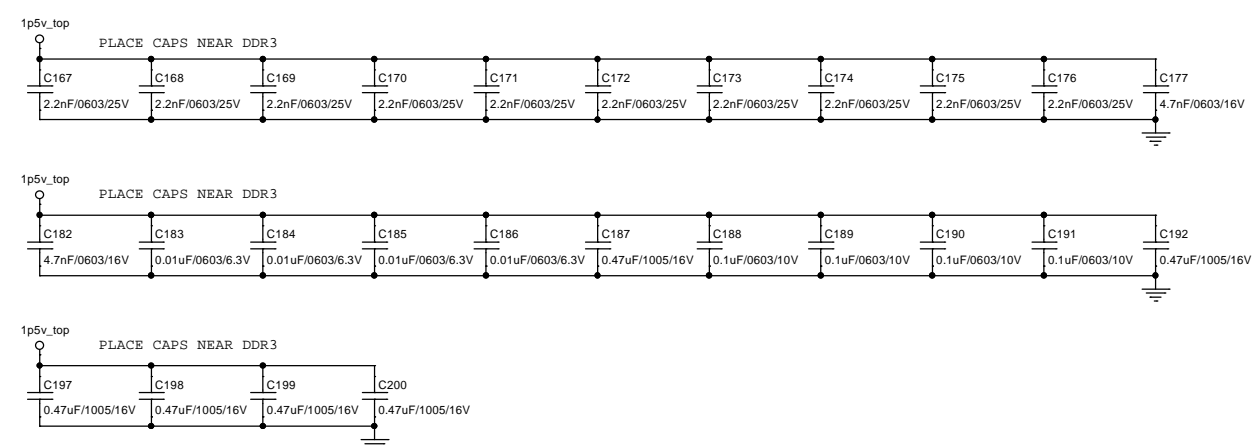
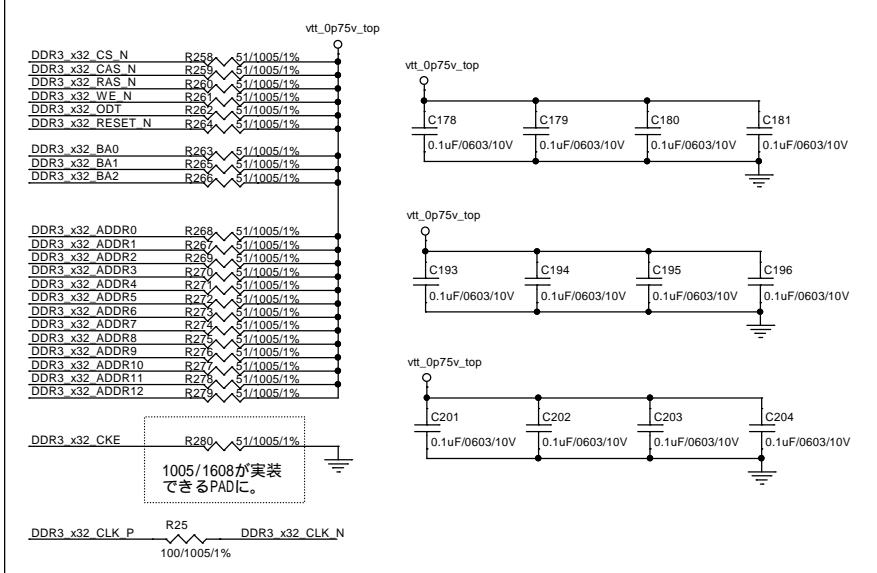
DDR3_x64_CLK1_P $\xrightarrow{R22}$ DDR3_x64_CLK1_N
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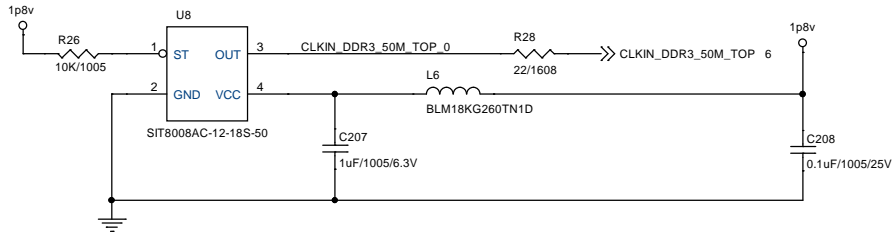


PLACE NEAR DDR3 DEVICES

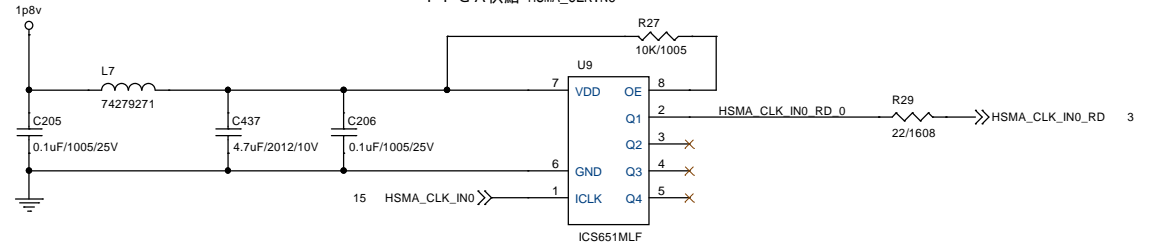


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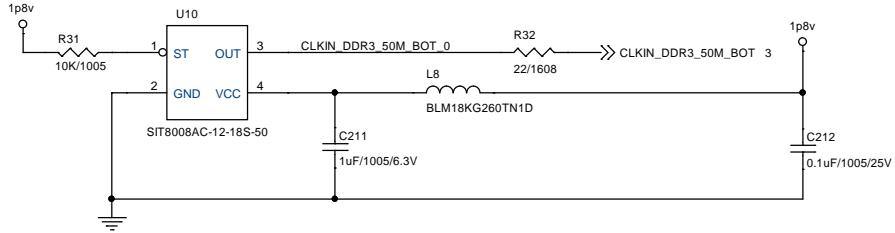
FPGA 供給50MHz (1.8V)



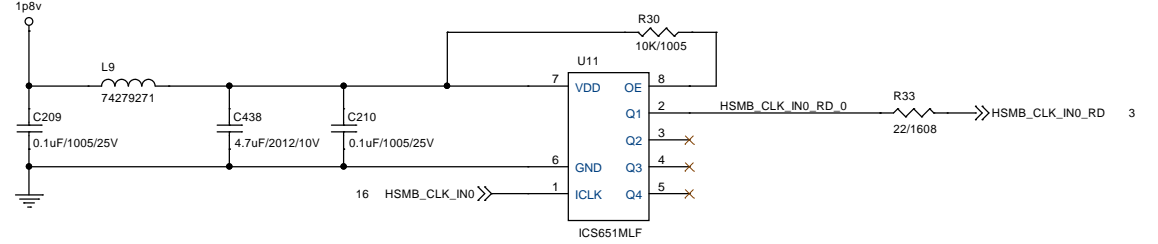
FPGA 供給 HSMA_CLKIN0



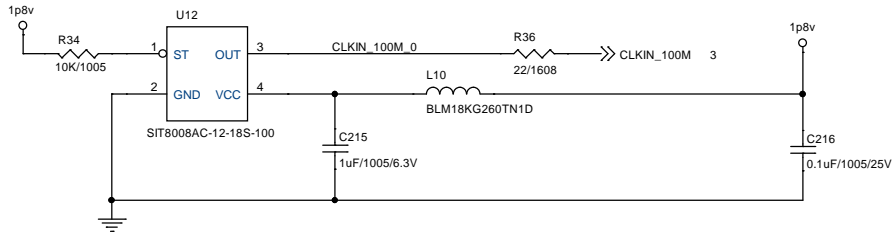
FPGA 供給50MHz (1.8V)



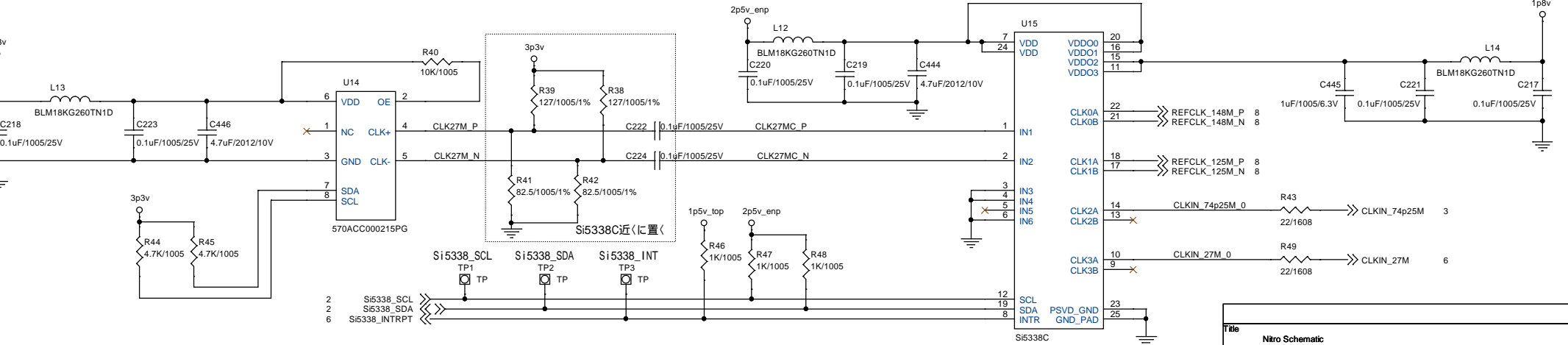
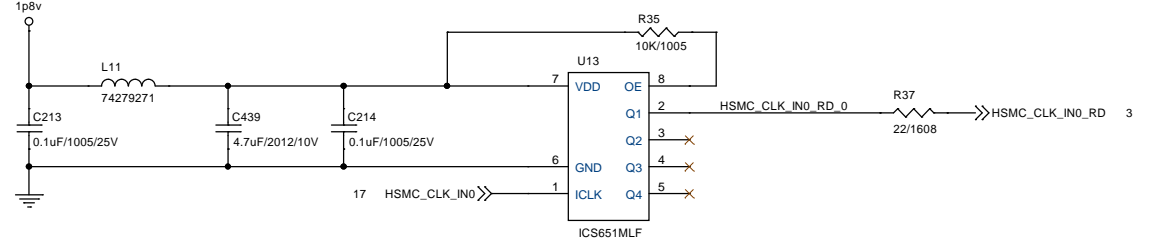
FPGA 供給 HSMB_CLKIN0



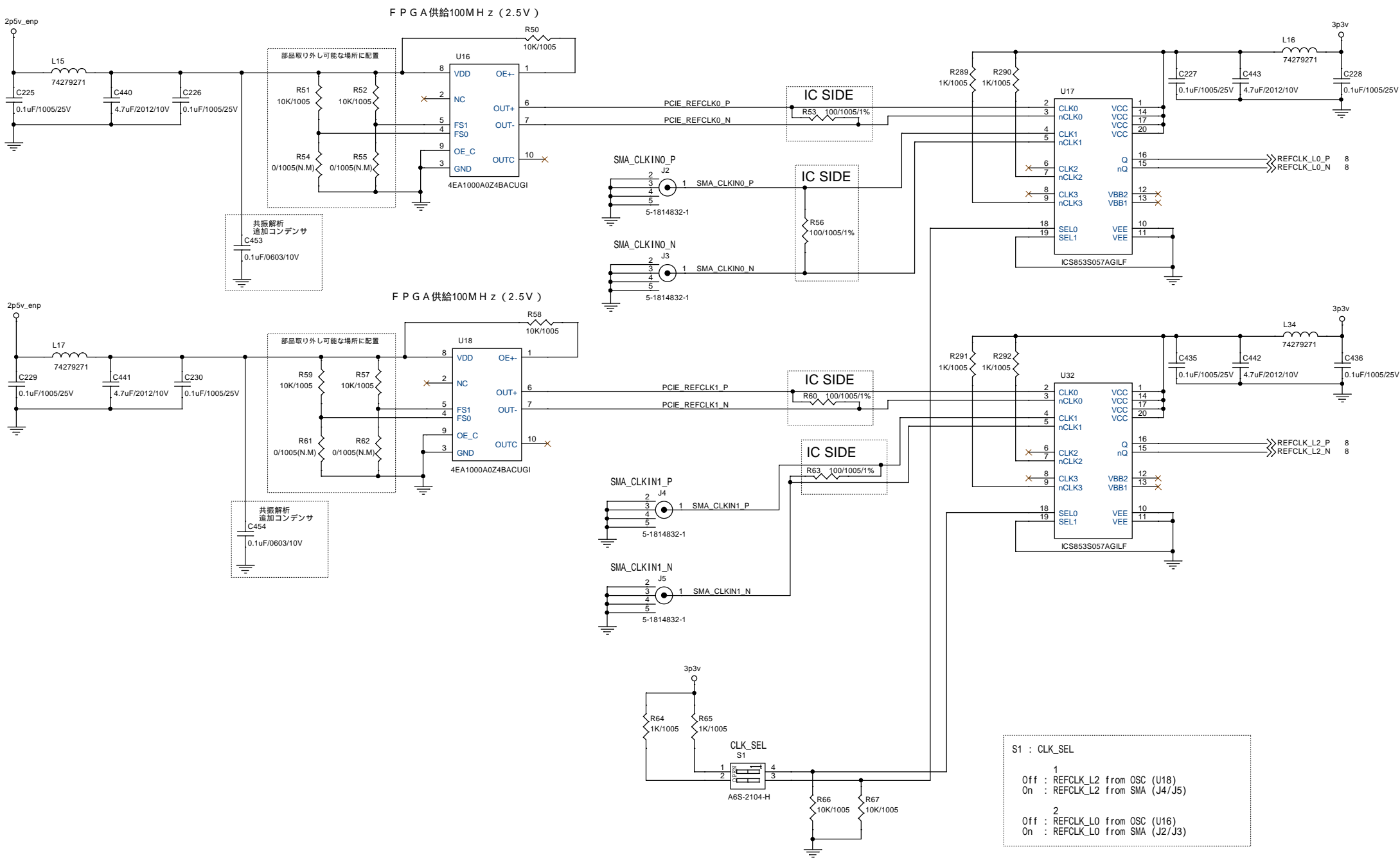
FPGA 供給100MHz (1.8V)



FPGA 供給 HSMC_CLKIN0



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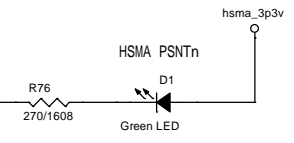
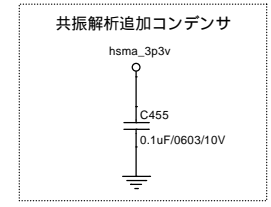
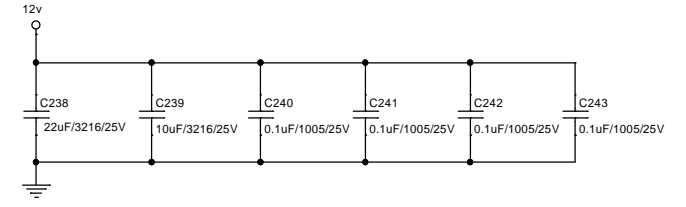
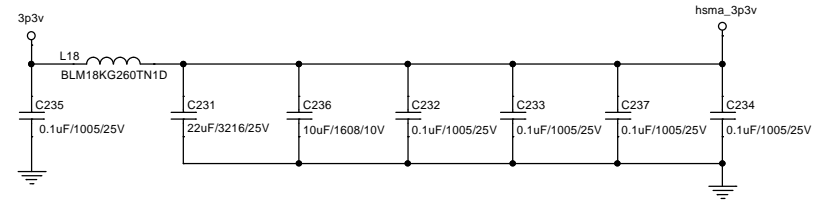
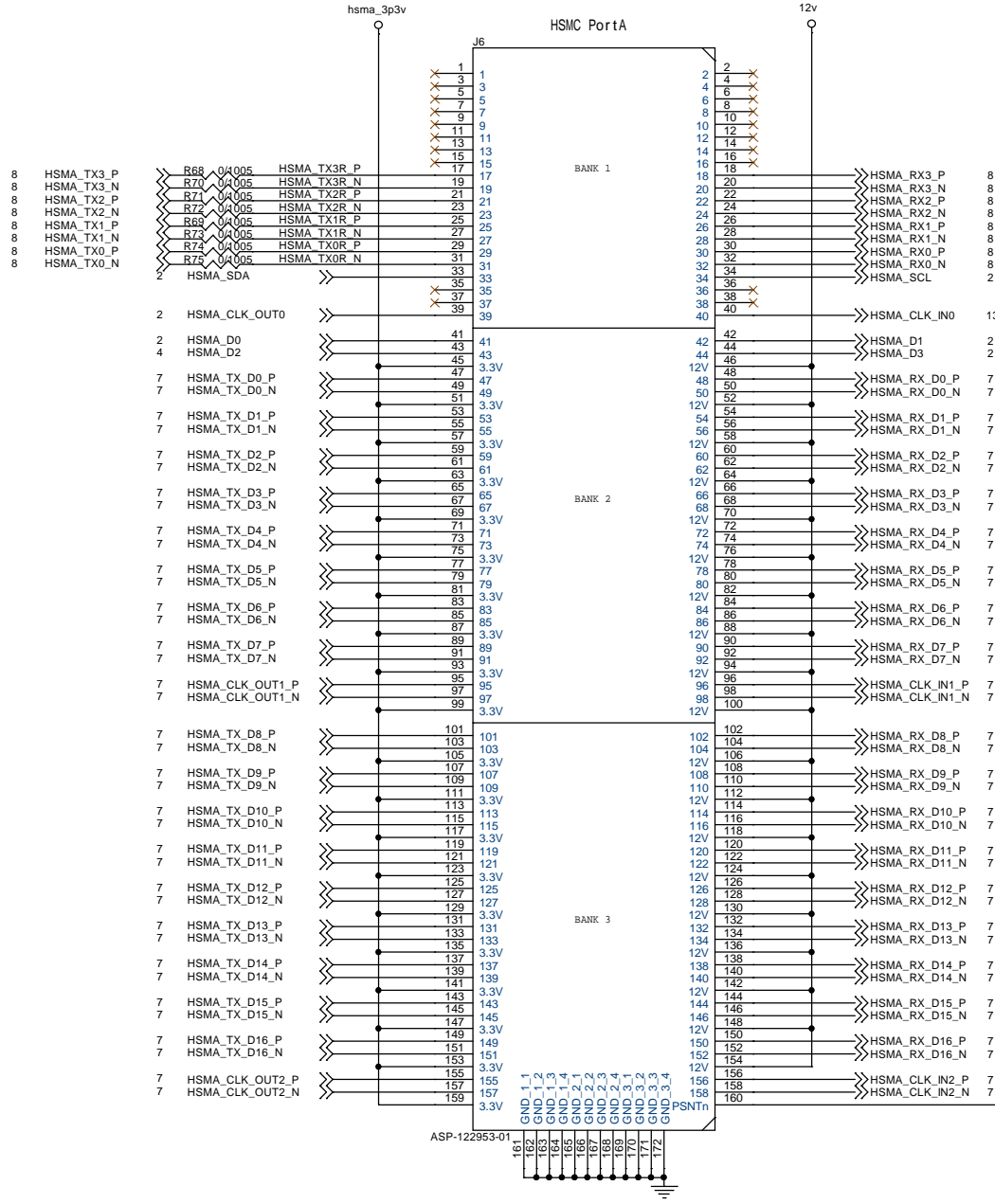


S1 : CLK_SEL

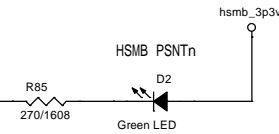
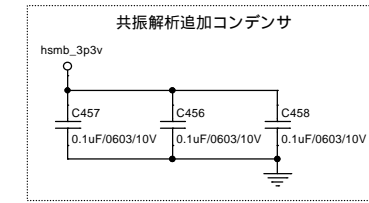
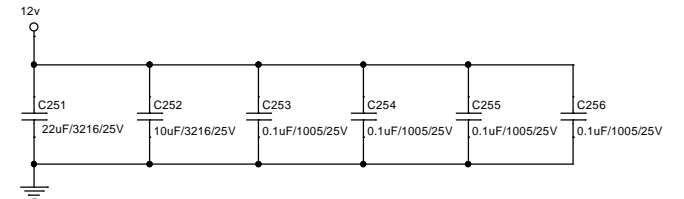
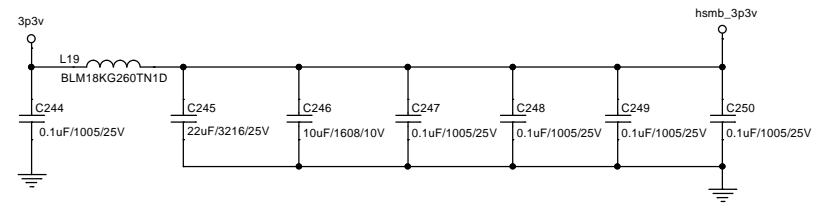
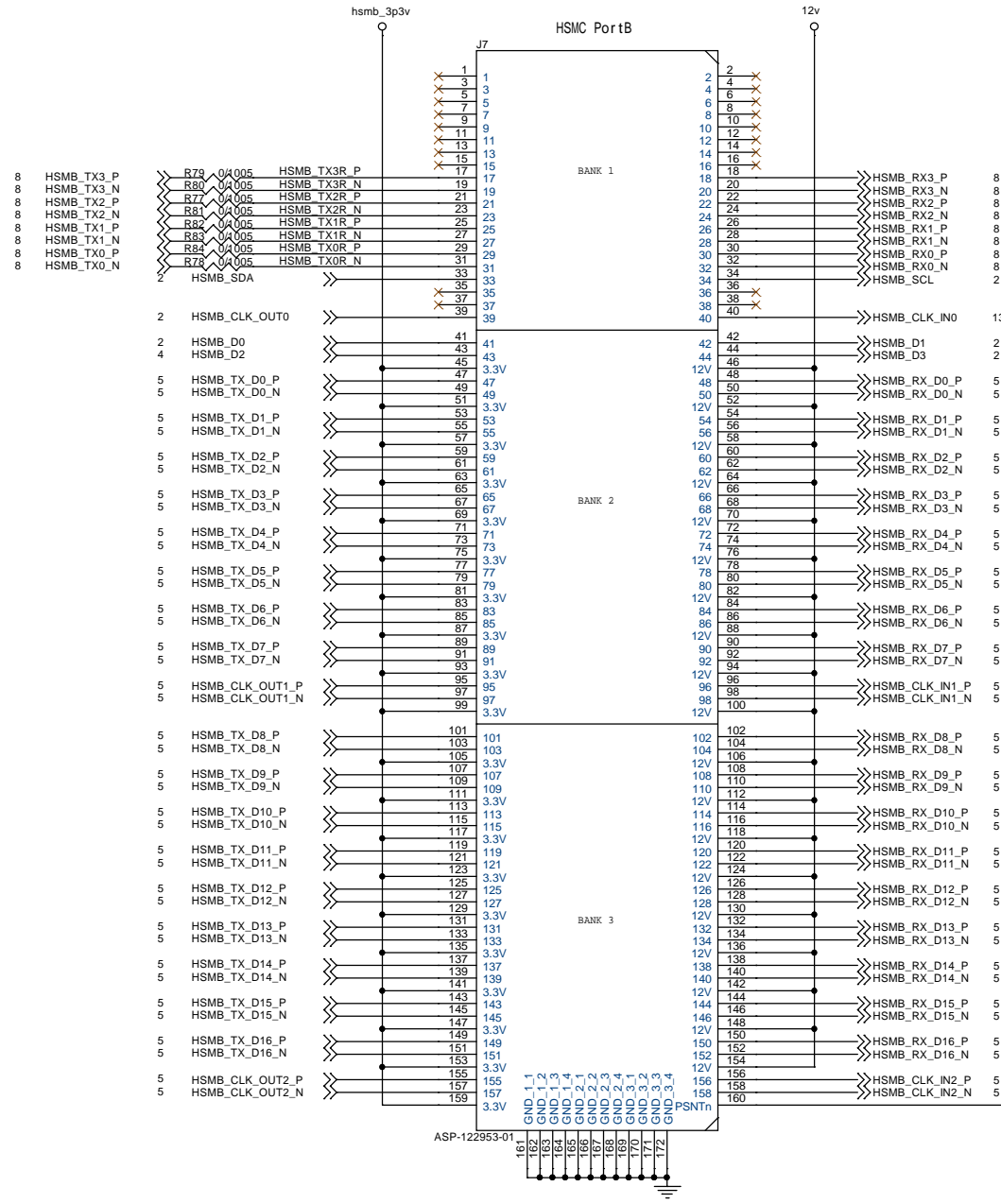
1
 Off : REFCLK_L2 from OSC (U18)
 On : REFCLK_L2 from SMA (J4/J5)

2
 Off : REFCLK_L0 from OSC (U16)
 On : REFCLK_L0 from SMA (J2/J3)

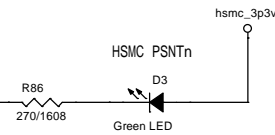
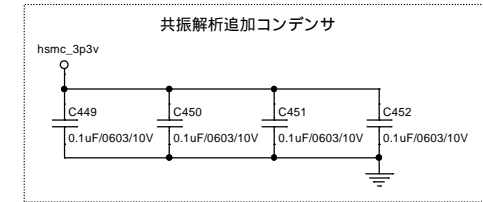
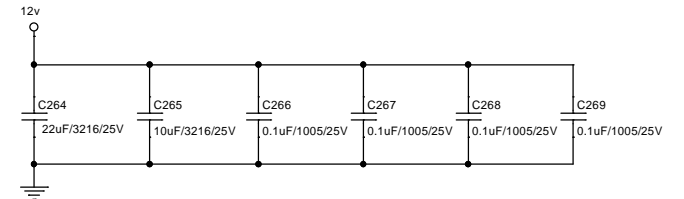
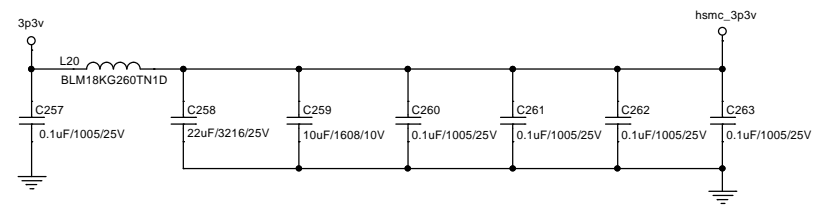
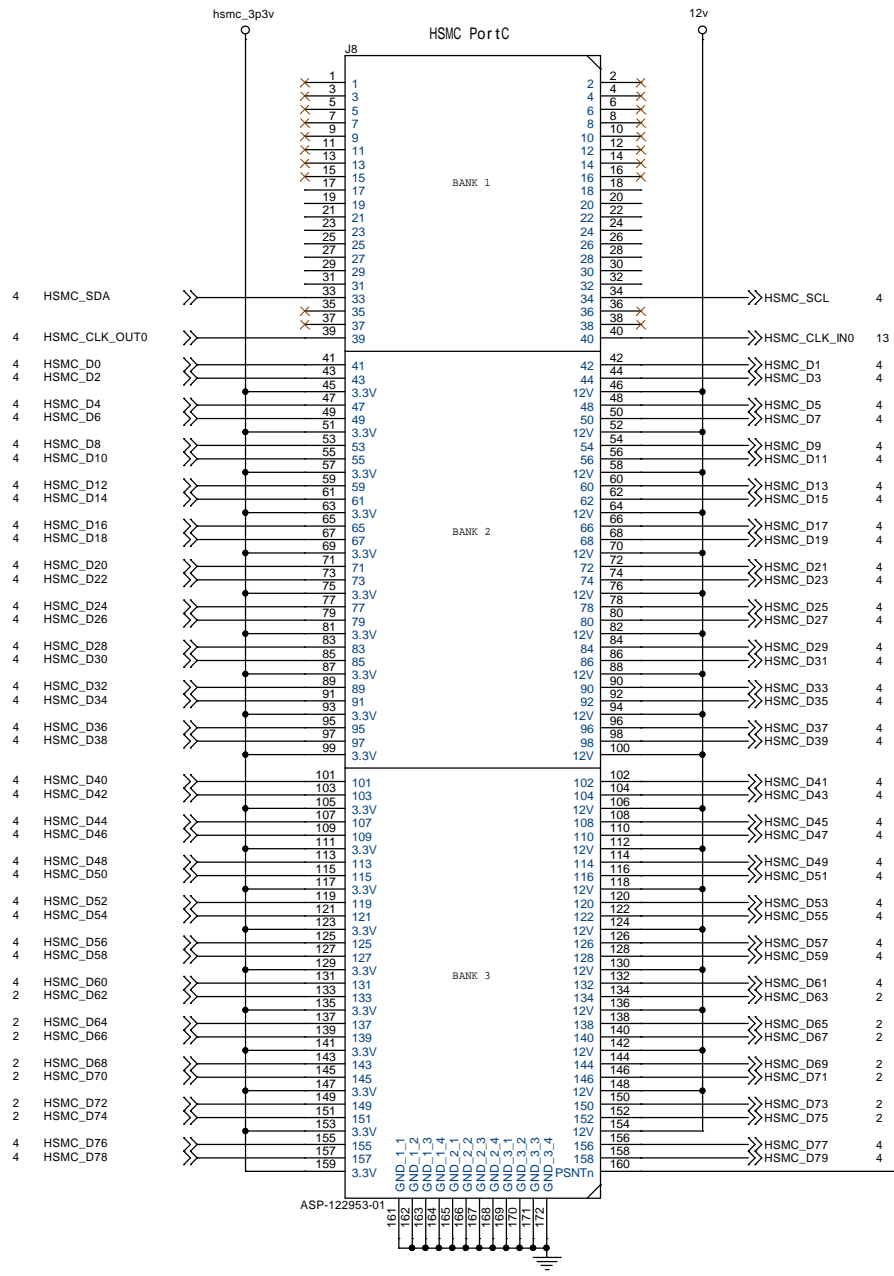
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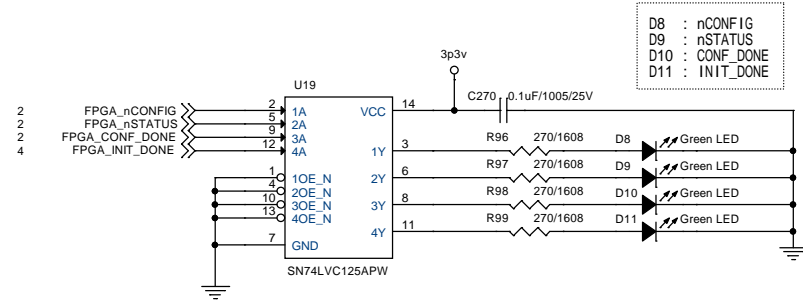
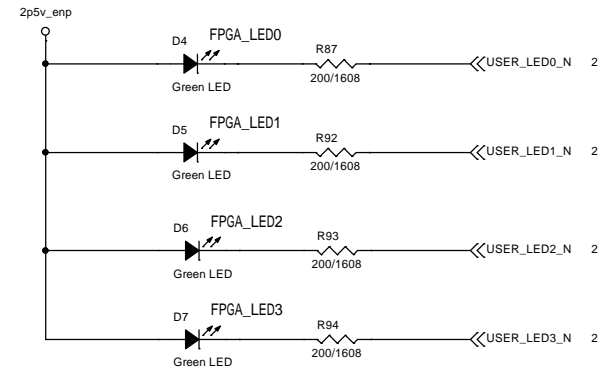
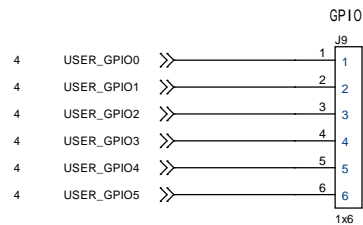
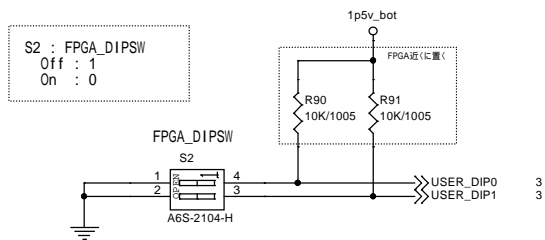
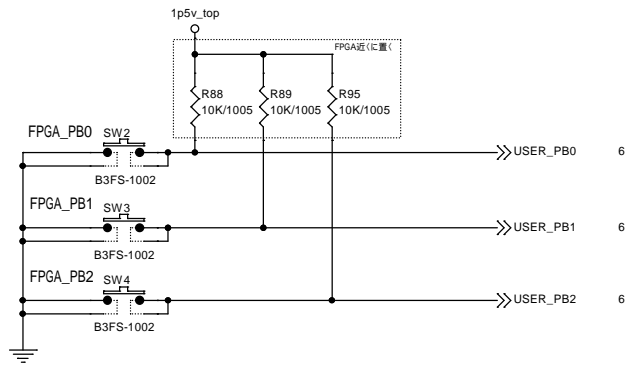
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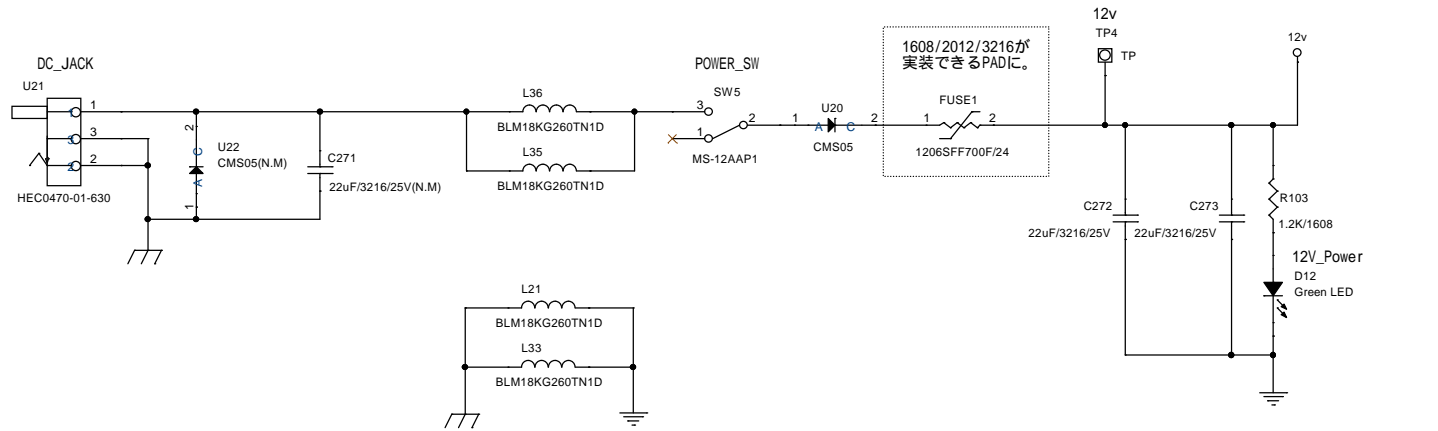


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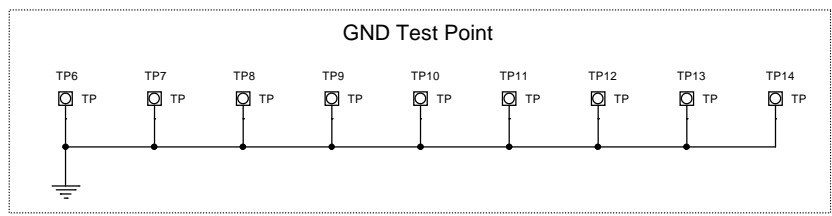
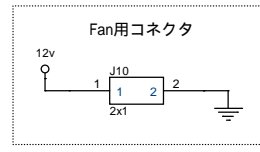
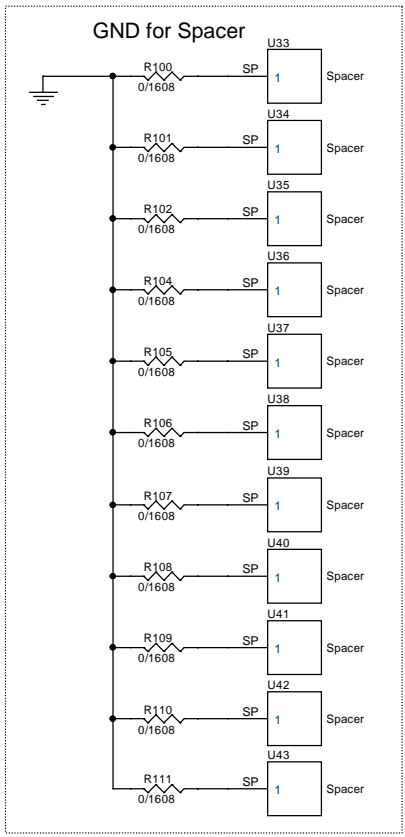
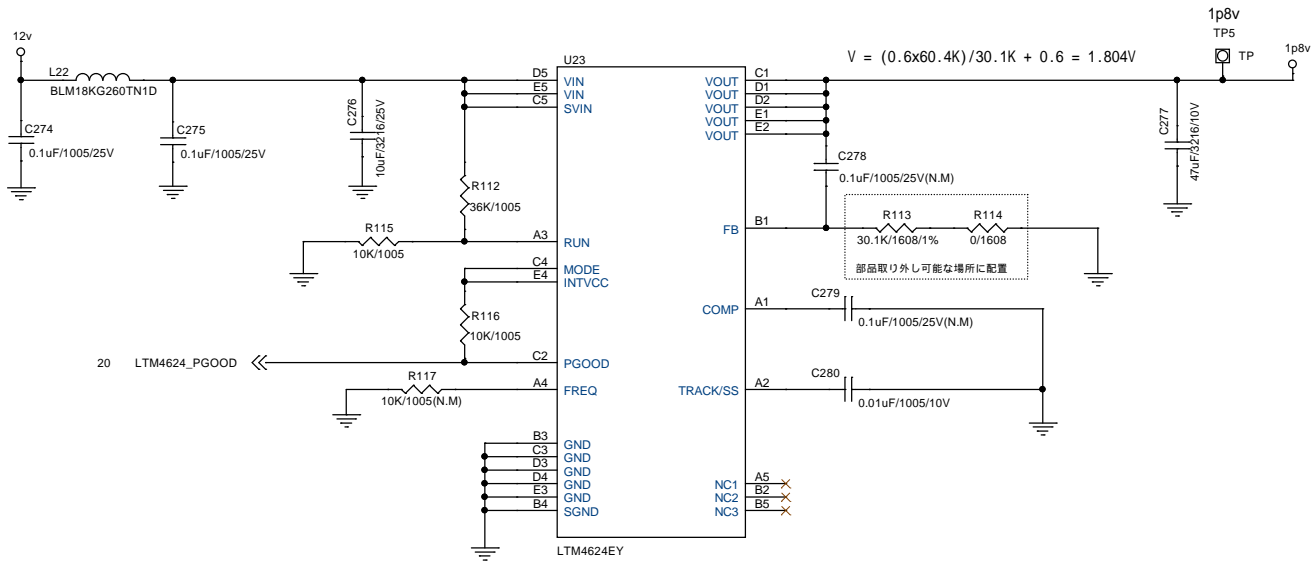


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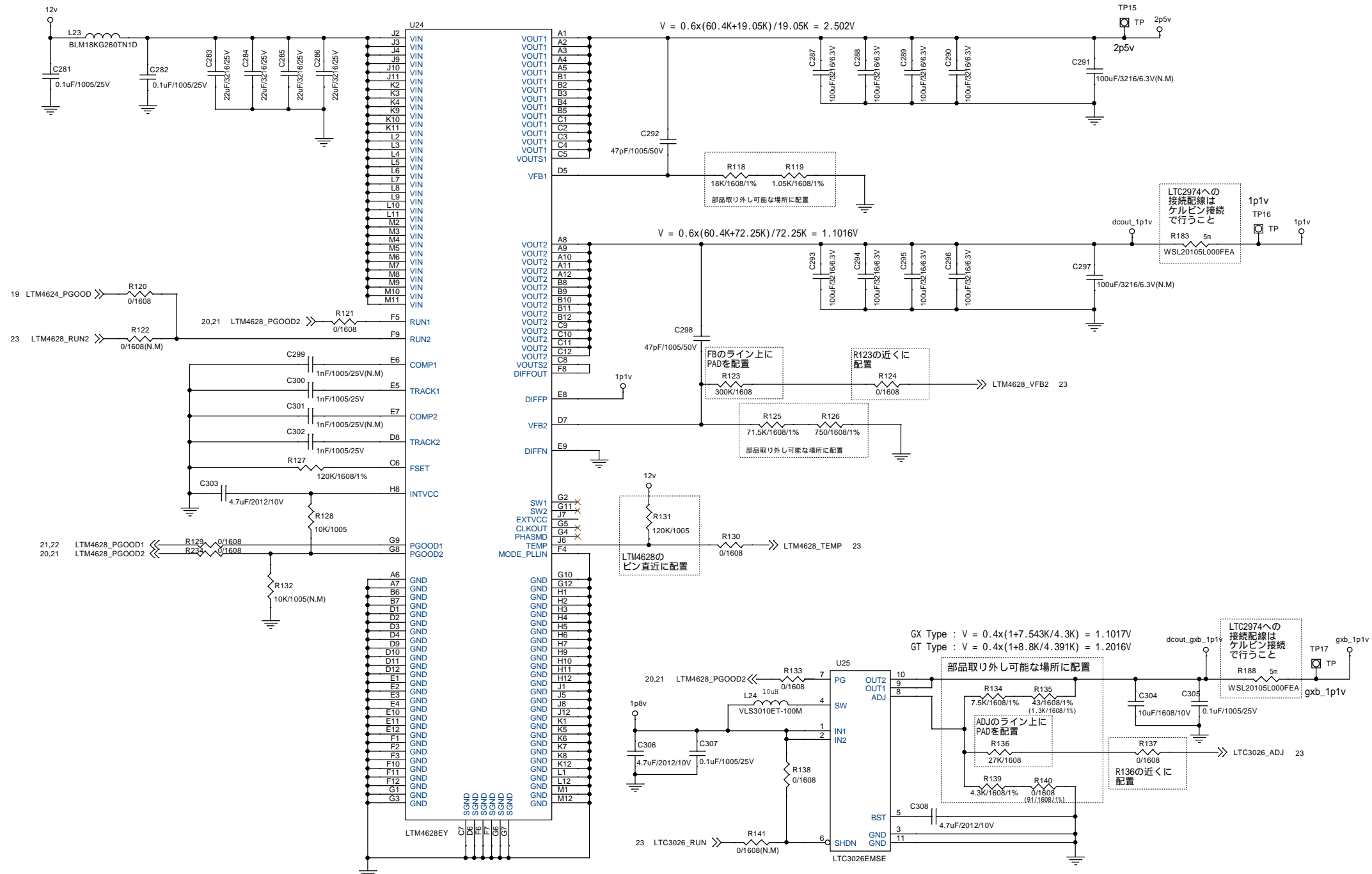




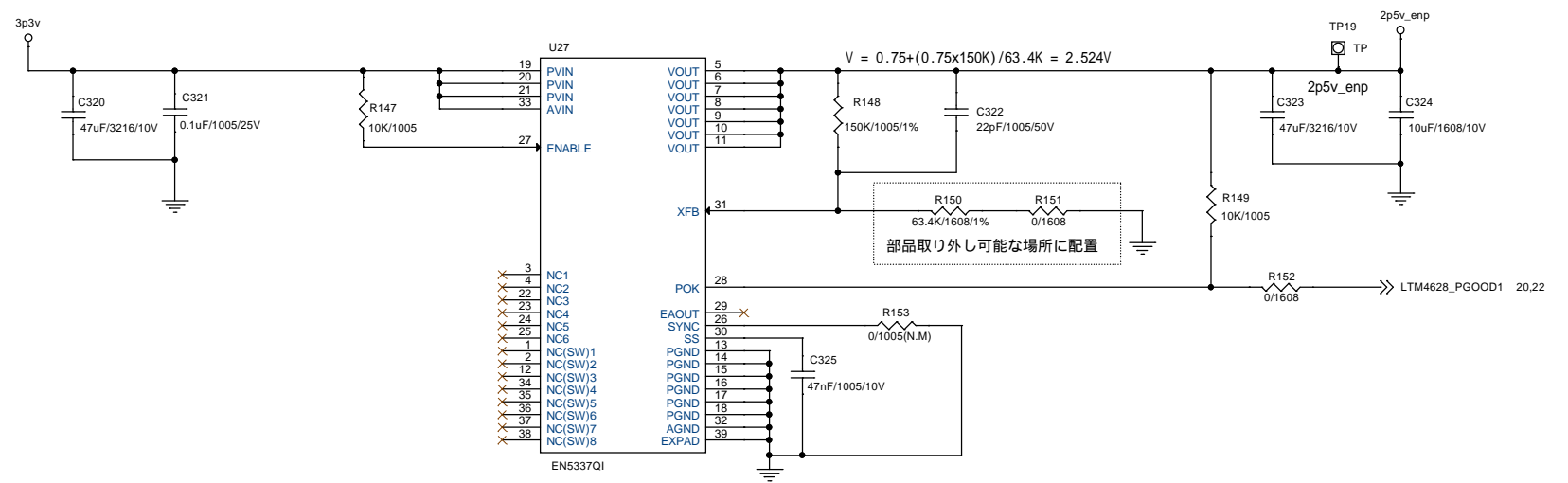
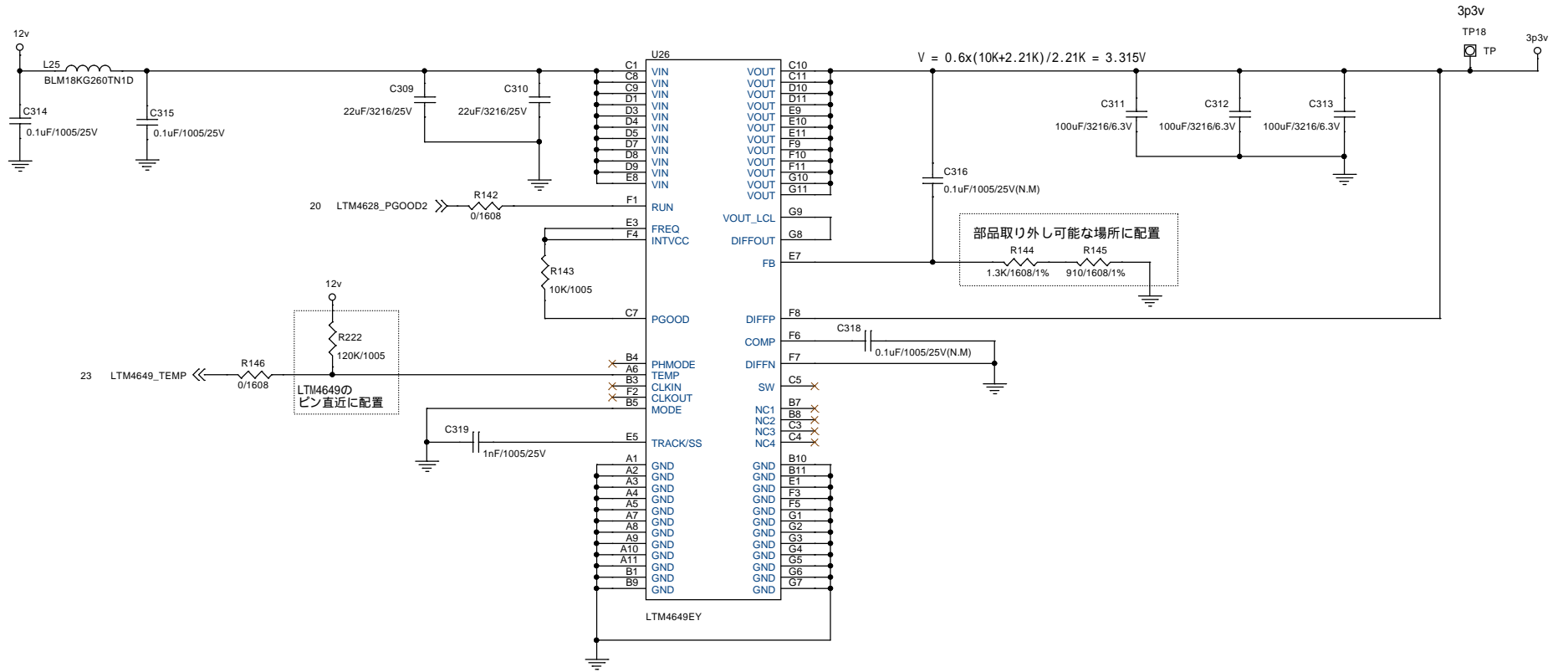
1608/2012/3216が
実装できるPADに。



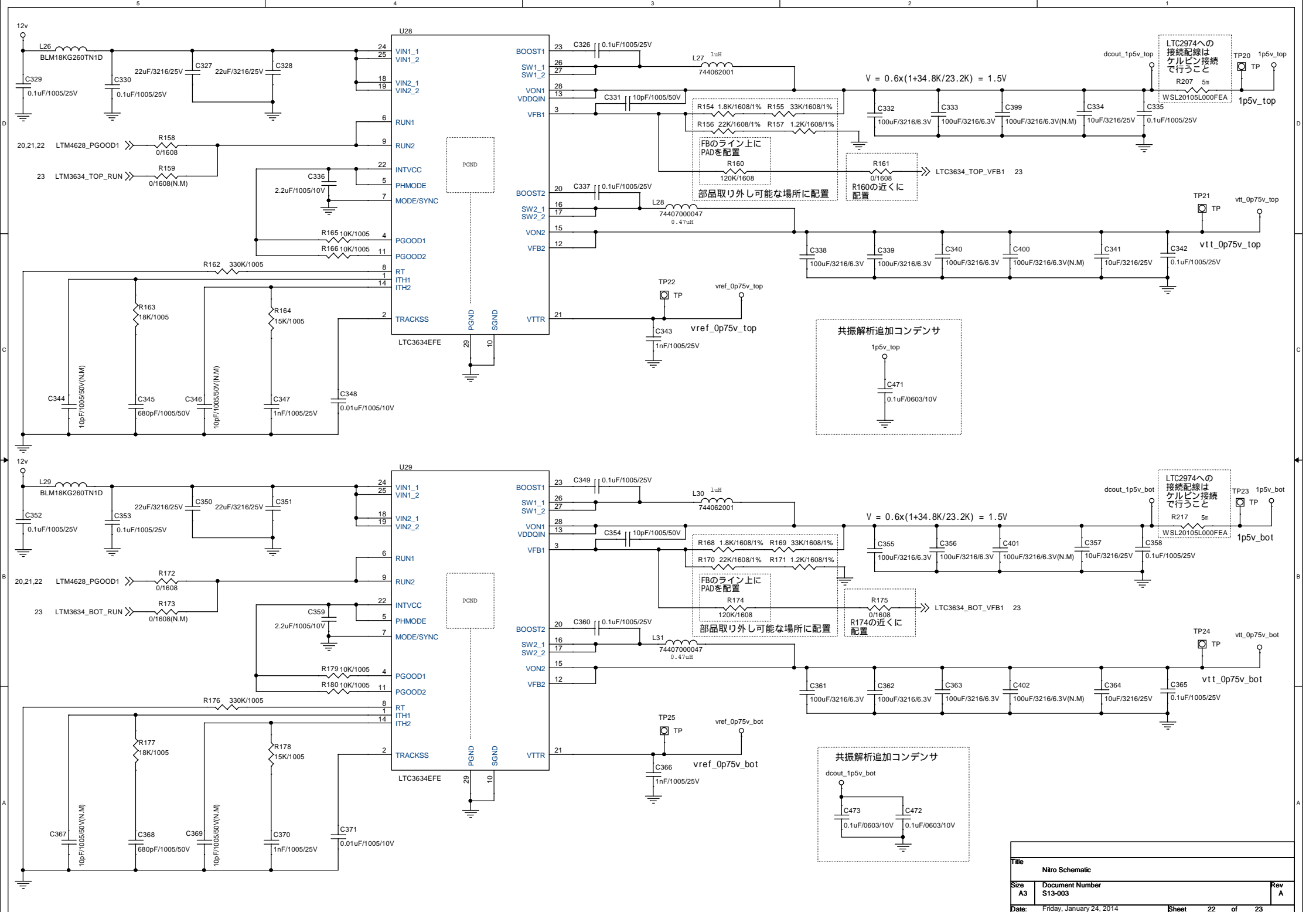
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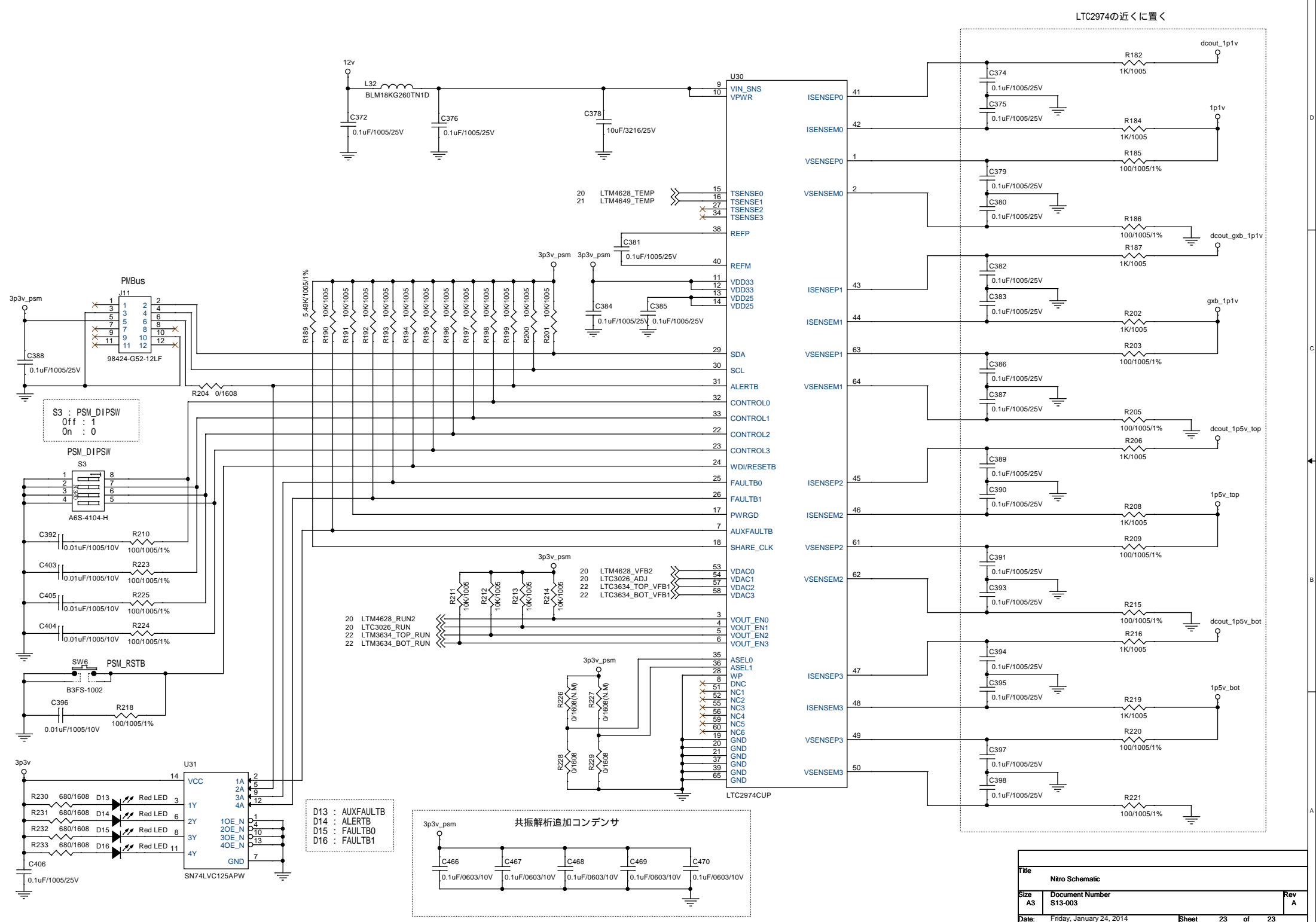
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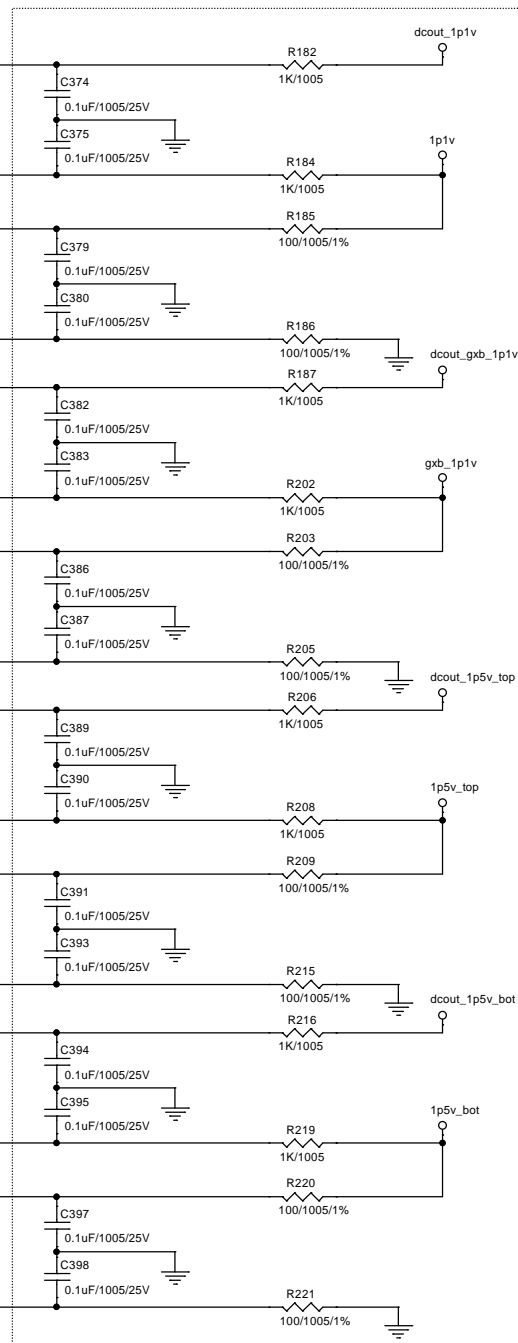
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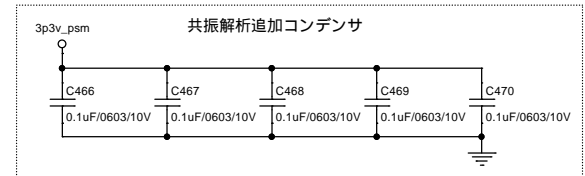
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D13 : AUXFAULTB
 D14 : ALERTB
 D15 : FAULTB0
 D16 : FAULTB1



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