Reference Manual

Mpression Magnes Board

Revision 1.0

2018/05/15

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1. Read This First

1.1. Important Information

READ FIRST:

- ***READ*** this Reference Manual before using this product.
- ***Keep*** this Reference Manual so you can refer to it when needed.
- ***Do not attempt*** to use this product until you fully understand its mechanisms.

Purpose of the Product:

- This product is intended to support development and verification of systems that use Arria10 GX from Intel. Using this system supports system development from both software and hardware aspects.
  Be sure to use this product correctly for this purpose.

For Users of This Product:

- This product should be used only by individuals who have carefully read and understand these materials and the Getting Started manual. Use of this product requires a basic knowledge of FPGAs, logic circuits, electronic circuits, and microcomputers.

Precautions to be taken when using This Product:

- This product is to be used for development of a program, and the evaluation stage. **You cannot install the board in your product** and cannot use the board for mass-production. When mass-producing a program you have finished developing, be sure to decide at your own responsibility whether it can be put to practical use by performing integration test, evaluation, or some other experiment.
- In no event shall Macnica Inc. be liable for any consequence arising from the use of this product.
- Macnica Inc. shall make effort to provide a workaround or fix for failures of this product, with or without charge. This does not mean, however, that Macnica Inc. guarantees to provide a workaround or fix under all circumstances.
- Macnica Inc. cannot anticipate every possible circumstance that might involve a potential hazard. The warnings in this reference manual and on the product are therefore not all-inclusive. Use this product correctly and safely at your own responsibility.
- Even if a device installed on this product has a failure, it cannot be replaced.
- The product is not guaranteed to operate with all peripheral USB devices.
- The product is not guaranteed to connect to the LAN interface or HDMI image output for all devices.
- Remodeling or damages caused by the customer is not guaranteed.
- This product is a lead-free mounting product.
- Generally, the brand names carried in this Getting Started each constitute a maker's trademark or registered trademark.

Improvement Policy:

- Macnica Inc. pursues a policy of continuous improvement in design, performance, and safety of the product. Macnica Inc. reserves the right to change, wholly or partially, specifications, design, reference manual, and other documentation at any time without notice.

Warranty:

- Macnica Inc. offers exchange of this product free of charge only in a set range of cases of initial trouble for this product, and within 30 days from when the customer received delivery of the Board. Macnica Inc. cannot exchange products in cases where breakdown is caused for the following reasons:
  (1) Misuse, abuse of the product or use under abnormal conditions
  (2) Remodeling or repair
  (3) A fire, earthquake, fall or other accidents

Figures:

- Some figures in this reference manual may differ from your system as purchased.

1.2. Developer Information

The Developer of this product is:
Macnica Inc.
1-6-3 Shin-Yokohama, Kouhoku-ku, Yokohama, 222-8561 JAPAN

1.3. Inquires

In case you have any inquiries about the use this product, please contact your local Macnica company or make inquiries through the contact form in the following web site:
http://www.m-pression.com/contact

Macnica companies:

• China & HK:	Cytech Technology	http://www.cytech.com/
• ASEAN & India:	Cytech Global	http://www.cytechglobal.com/
• Taiwan:	Galaxy Far East Corp.	http://www.gfec.com.tw/
• North America:	Macnica Americas	http://www.macnica.com/americas/
• Brazil:	Macnica DHW	http://www.macnicadhw.com.br/en/
• Japan:	Altima	http://www.alt.macnica.co.jp

2. For Ensuring Safe Use

Be sure to follow the precautions given here, which are intended to prevent harm to the user and others, as well as material damage.

2.1. Legend

Danger	Indicates an imminent hazardous situation which if not avoided will result in death or serious injury.
Warning	Indicates a potentially hazardous situation which if not avoided could result in death or serious injury.
Caution	Indicates a potentially hazardous situation which if not avoided may result in minor or moderate injury or in property damage.

- **Notes and important information** are used to inform users about exceptional conditions, cautions for operational procedures, and in explanations.

2.2. Cautions

Danger	Be sure to use the AC adapter (included in the package), which meets the specifications described in this Manual. Using an AC adapter not meeting the specifications described in this Manual may cause the kit to emit heat, explode, or ignite.
Warning	Do not apply strong impacts or blows to the kit. Doing so may cause the kit to emit heat, explode, or ignite, or the equipment in the kit to fail or malfunction. This may also cause fire.
	Do not put the main unit or the AC adapter in cooking appliances, such as microwave ovens, or high-pressure containers. Doing so might cause the main unit or AC adapter to emit heat, explode, ignite, or emit smoke, or its parts to break or warp.
	Do not wrap the main unit that is in use with cloth or other materials that are likely to allow heat to build up inside the wrapping. This will cause heat to build up inside the wrapping which may cause the main unit to ignite or malfunction.
	When disposing of the main unit, do not dispose of it along with general household waste. Throwing the main unit into fire may cause it to explode. Dispose of the main unit following the laws, regulations, and ordinances governing waste disposal.
	Do not pull the power supply cable with excessive force or place heavy items on it. Do not damage, break, bundle, or tamper with the power supply cable. Damaged parts of the power supply cable might cause a short circuit resulting in fire or accidents involving electrical shock.
	Do not plug or unplug the power plug with wet or moist hands. This might cause injuries or equipment malfunctions or failures due to electrical shock.
	Plug the power plug securely into the outlet. If the power plug is not securely plugged into the outlet, it may cause electrical shock or fire due to the electricity that is emitted.

Warning (Continued from previous page)	Do not connect many electrical cords to a single socket or connect an AC adapter to an outlet that is not rated for the specified voltage. Doing so may cause the equipment to malfunction or fail, or lead to accidents involving electrical shock or fire due to the heat that is emitted.
	Periodically remove any dust accumulated on the power plug and around the outlet (socket). Do not use a power plug with dust accumulated on it because doing so will lead to insulation failure due to moisture which may lead to fire. Remove any dust on the power plug and around the outlet with dried cloth.
	Do not place any containers such as cups or vases filled with water or other liquid on this Board. If this Board is exposed to water or other liquids it may cause the Board to malfunction or lead to accidents involving electrical shock. If you spilled water or other liquid on this Board, immediately stop using the Board, turn off the power, and unplug the power plug. If you have any requests for repairs or technical consultation, please contact the local Macnica company or Mpression inquiry URL.
	Keep this board and accessories out of reach of children. Failure to do so may lead to injuries.
Caution	Do not place the kit on unstable places such as shaky stands or tilted locations. Doing so may cause injuries or cause this Board to malfunction if the Board should fall.
	Do not attempt to use or leave the kit in places subject to strong direct sunlight or other places subject to high temperatures such as in cars in hot weather. Doing so might cause the kit to emit heat, break, ignite, run out of control, warp, or malfunction. Also, some parts of the equipment might emit heat causing burn injuries.
	Do not use the kit in places subject to extremely high or low temperatures or severe temperature changes. Doing so may cause the kit to fail or to malfunction. Always be sure to use the kit within a temperature range of 5°C to 35°C and a humidity range of 0% to 85%.
	Unplug the power supply cable when carrying out maintenance of devices in which the main unit is embedded. Failure to do so may lead to accidents involving electrical shock.
	Do not place this board in locations where excessive force may be applied to it. Doing so may cause the PC board to warp, leading to breakage of the PC board, missing parts or malfunctioning parts.
	When using the kit together with expansion boards or other peripheral devices, be sure to carefully read each of their manuals and to use them correctly. Developer does not guarantee the operation of specific expansion boards or peripheral devices when used in conjunction with this Board unless they are specifically mentioned in this Manual or their successful operation with this Board has been confirmed in separate documents.
	Be sure to turn off the power switch when moving this Board to connect to other devices. Failure to do so may cause this Board to fail or lead to accidents involving electrical shock.
	Do not clean this Board by using a rag containing chemicals such as benzine or thinner. Failure to do so will likely to cause this Board to deteriorate. When using a chemical cloth be sure to comply with any directions or warnings.

Caution (Continued from previous page)	Do not immediately turn on the power if you find that water or moisture had condensed onto the main unit after removing the board from the package. Condensation might occur on this Board when taking it out of the box, if the board is cool yet the room temperature is warm. Do not apply power to the Board while water or moisture has condensed on it because the moisture may cause the Board to break or may shorten the service life of the parts. When you first take this Board out of the box be sure to leave it at room temperature for a while before using it. If condensation or moisture has occurred on this Board, first wait for the moisture to fully evaporate before installing or connecting the Board to other devices.
	Do not disassemble, dismantle, modify, alter, or recycle parts unless they are clearly described as customizable in this Manual. Although this board is a customizable product, overall product operation cannot be guaranteed if parts needed for basic operations, which are not specified in this Manual as customizable, are modified in any way. Please contact the local Macnica company or Mpression inquiry URL beforehand if you wish to customize or modify any parts that are not described in this Manual as customizable.

3. Unboxing

When unpacking the product, make sure that everything is included and that nothing is damaged. If something is missing, or if you discover physical damage, contact your sales representative within 30 days after the product was delivered to you.

Magnes	1
AC adapter (12 V/16.7 A)	1
Spacers for board mounting	6 sets
Heat sink	1
Guide for Developers	2
Circuit diagram of the product	Download these files from the website at the URL noted in “Guide for Developers”.
Reference Manual	
Getting Started	

Caution	Consider using the heat sink provided if the usage conditions or the environment cause the FPGA to heat up. Note that when you attach the heat sink, the heat transfer sheet (sticker) sticks it to the FPGA. Be careful, because forcefully removing it may damage or break the board. The heat sink is equipped with a cooling fan. Connect the power cable of the cooling fan to CN23 on the product. For details, refer to section 7.2.9. Further, please note that we bear no responsibility for damage or breakage caused by attaching or removing it.

4. Functions and Features of the Product

4.1. Features

This board is an excellent platform for hardware engineers and software developers because it is equipped with an Intel® Arria® 10 GX FPGA, has two FPGA Mezzanine Card (hereafter FMC) connectors, and has a COM Express® (hereafter COMe) connector to provide both high expandability and flexibility. This board is equipped with two banks of 2-GByte DDR4-SDRAM and an HDMI, and two high-speed mezzanine connectors capable of configuring up to two expansion cards, either commercially available or self-developed. In addition, the COMe connector and FPGA are connected by PCIe (Gen2), so an all-purpose CPU can be easily connected while FPGA + CPU configurations allow development of a variety of applications.

For more detailed information and other related materials about the FPGA equipped on the board, visit the link below.

- Intel® Arria® 10 FPGA

4.2. Key Components

The board's product specifications are shown below.

Key components	ALTMAGNESA10GX
Power	DC12V 16.7A AC adapter and ATX power input specifications Turn power on/off with slide switch
External Dimensions	244 mm x 190.5 mm
Board	12-layer through-hole FR-4
Operating Conditions	Temperature: 5°C to 35°C, Humidity: 0% to 85% (no condensation)
FPGA side	
Equipped FPGA	10AX090N2F40E2SG
Configuration ROM	EPCQL1024
Memory	DDR4-1866(933 MHz) 32 bits x2 banks
Clock	Clock Generator: Si5340B-D08017-GM -233.33 MHz, 233.33 MHz, 100 MHz Si5340B-D08111-GM -100 MHz, 100 MHz, 125 MHz, 148.5 MHz Si5340B-D08427-GM -100 MHz, 270 MHz, 270 MHz Oscillator: C7L-48000-080-BQ4-J7 -48 MHz 570BCC001868DG -48 MHz
JTAG	DIP 10-pin Header 2.54-mm pitch
Peripheral interface	・HDMI Type-A output connector x1 ・USB-UART USB Standard-B connector x1 ・FMC connector High pin count x1, Low pin count x1 ・COMe connector x1 COMe module Type-6, compact type, can be equipped PCI Express Gen2 x4 lane
User interface for debugging	・LED x8 (red x4, green x4) ・8bit DIP Switch x1 ・Push Switch x4 ・FAN connector
COMe side	
Peripheral interface	・PCI Express Gen2 x4 lane for FPGA ・Gigabit Ethernet RJ45 connector x1 ・USB3.0 connector x4 ・HDMI output connector x1 ・SATA connector x1 ・CPU FAN control connector ・Coin battery holder for RTC

4.3. Block Diagram

The board's block diagram is shown below.

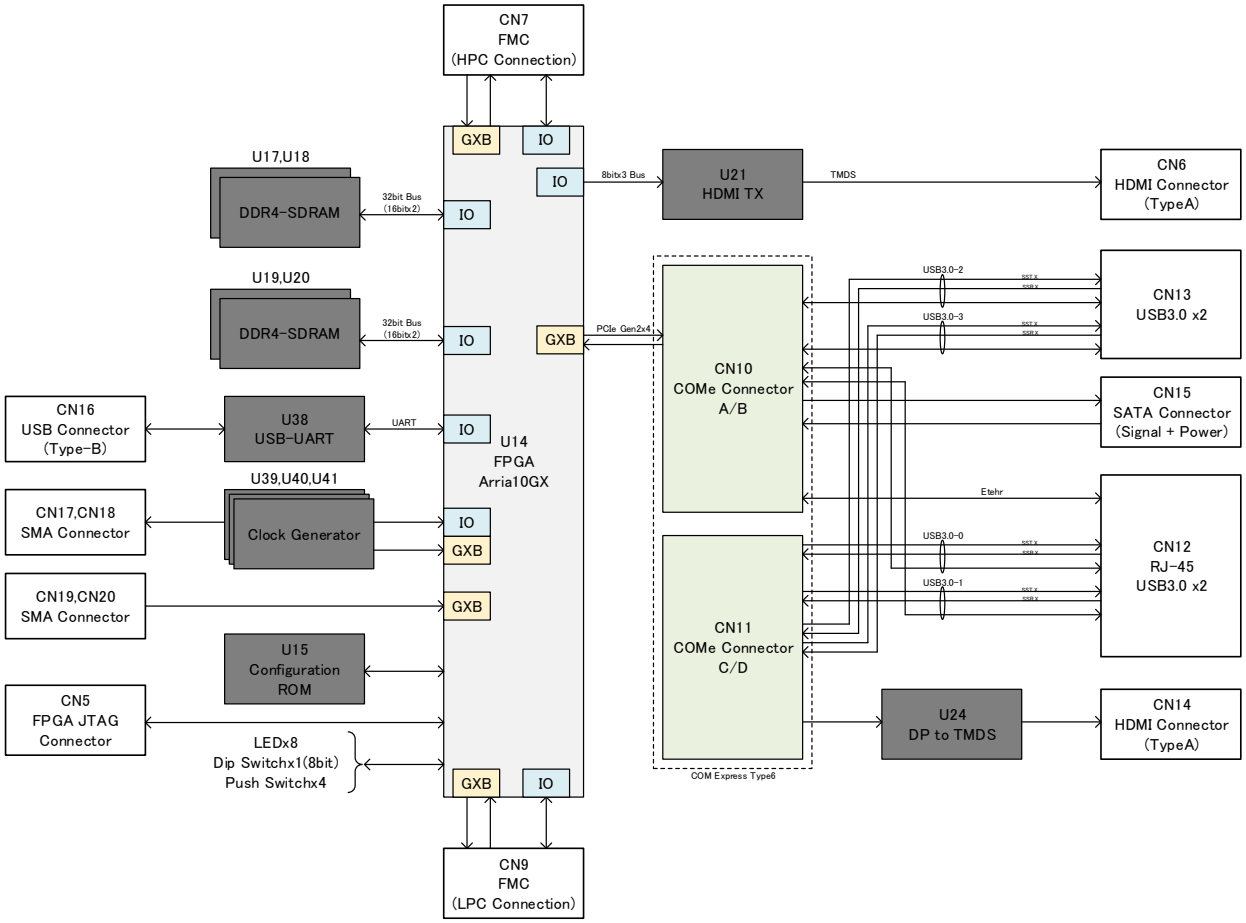

Figure 4-1 General Block Diagram

5. External View of Board

The external view of the board is shown below.

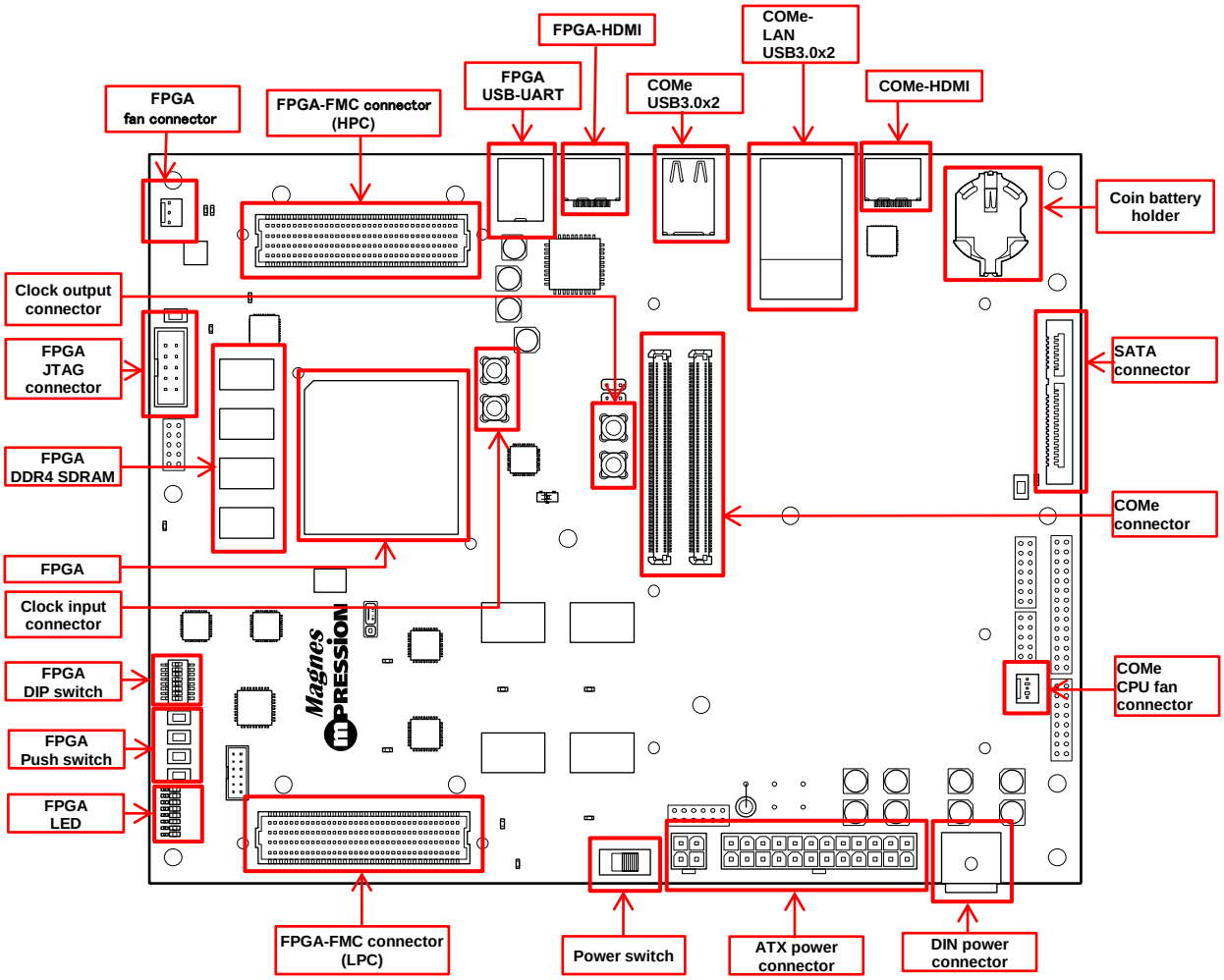

Figure 5-1 External View of Board (Components Side)

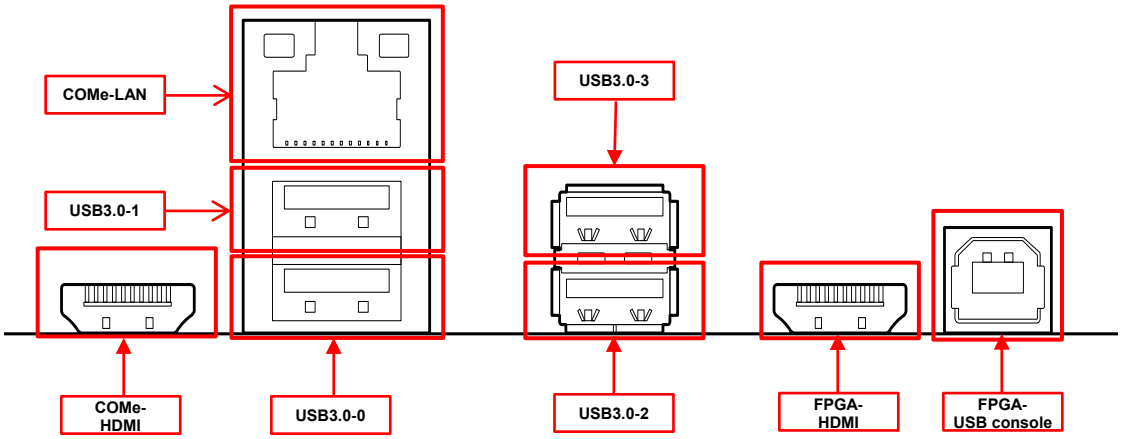

Figure 5-2 External View of Board (Profile of Connector Side)

6. Board Specifications

The major specifications of the board are shown below.

Table 6-1Board Specifications

Item	Specifications
External Dimensions	W: 244 mm x H: 190.5 mm
Layer configuration	12 layers
Board thickness	2.0 mm
Material	FR-4

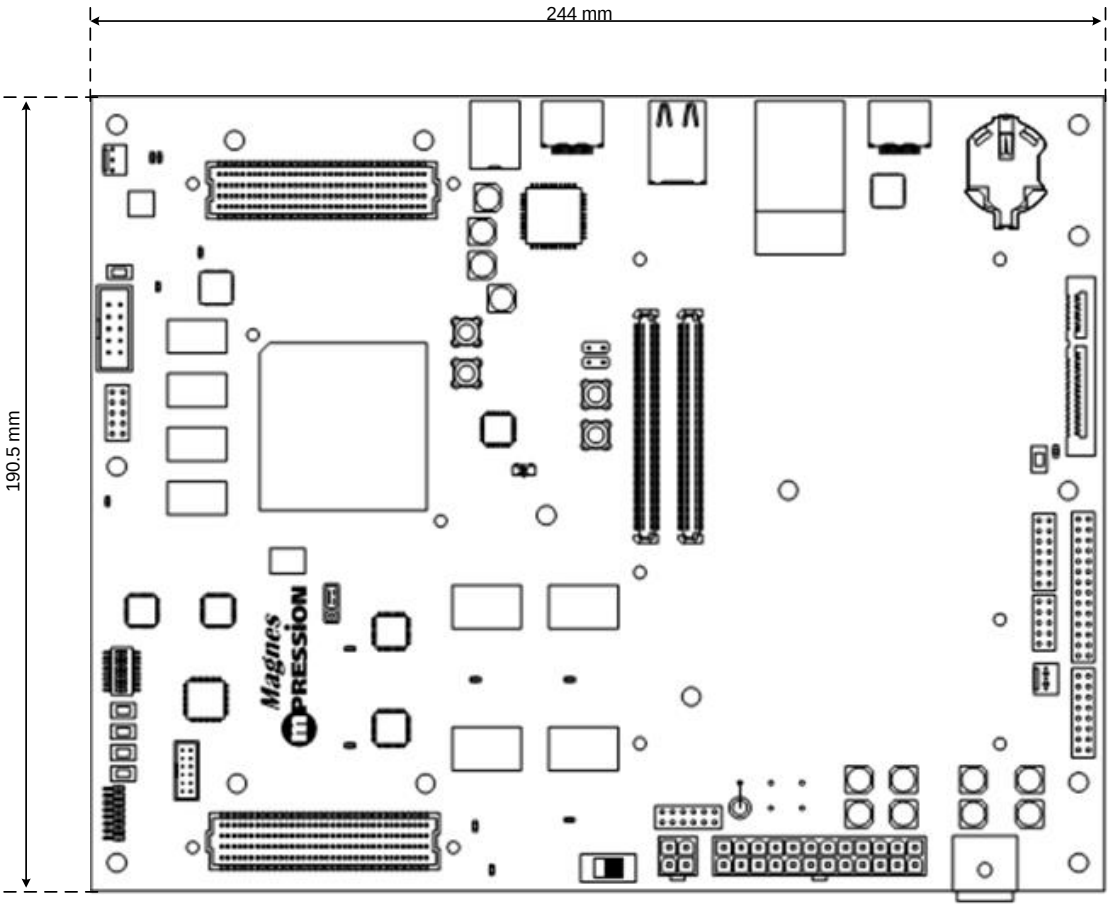

Figure 6-1Board Dimensions

7. Explanation of Components

7.1. Power Supply Configuration

This board is equipped with a 24-pin connector to connect an ATX power supply for power input and a DIN connector for the AC adapter. The board uses +12 volts from the ATX power supply or the AC adapter.
The startup timing of the power supply ICs are controlled through the power supply control IC (U3). A connector (CN4) is also equipped for the PMBus controller and the power supply control IC, so it is possible to monitor the voltage and control the various power supply ICs through the power supply control IC from a PC.
You can check the operation of the power supply generated on the board through LEDs 12 through 22.

An overview of the power supplies is shown in the following block diagram.

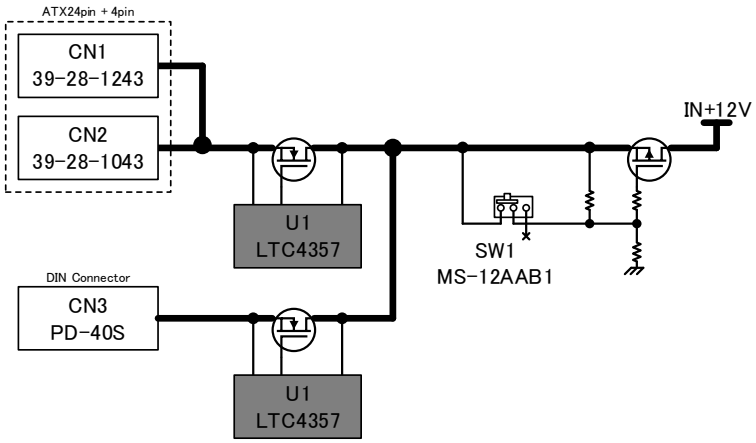

Figure 7.1-1 Power Input Block Diagram

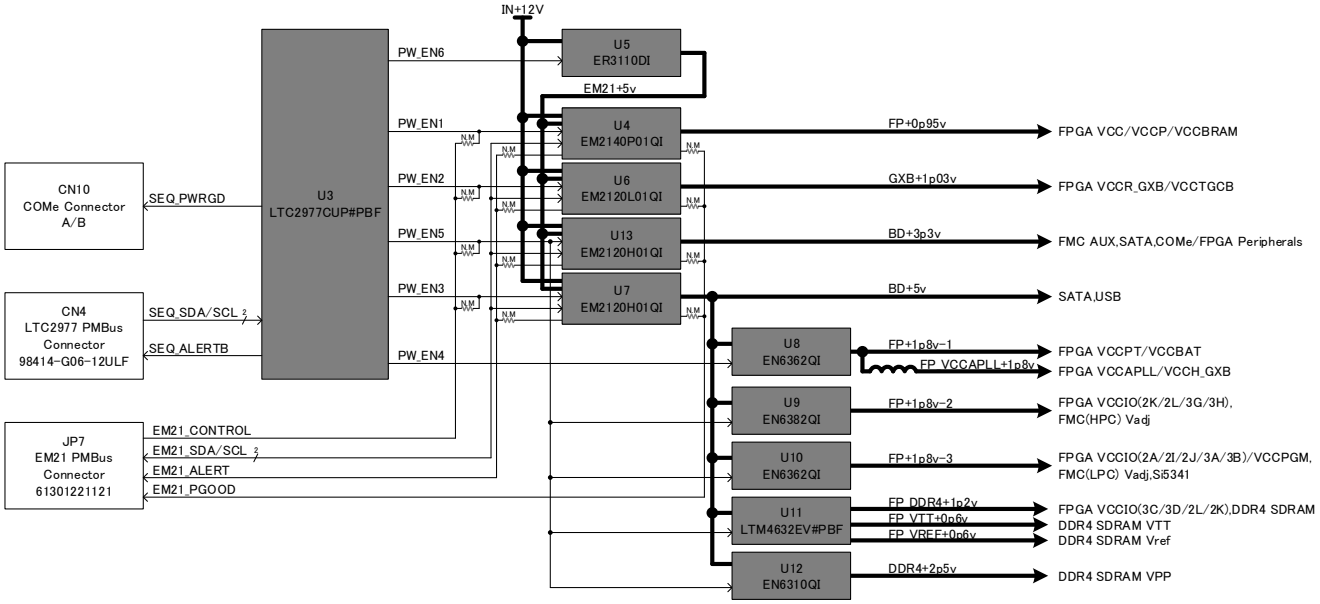

Figure 7.1-1 Internal Power Supply Block Diagram

7.1.1.Power Input Components

The ATX power supply (CN1) and DIN connector (CN3) for the AC adapter are shown below.
To use the board, you need to supply + 12 volts from one of these connectors.
* The CN2 is an ATX 12 V expansion connector.

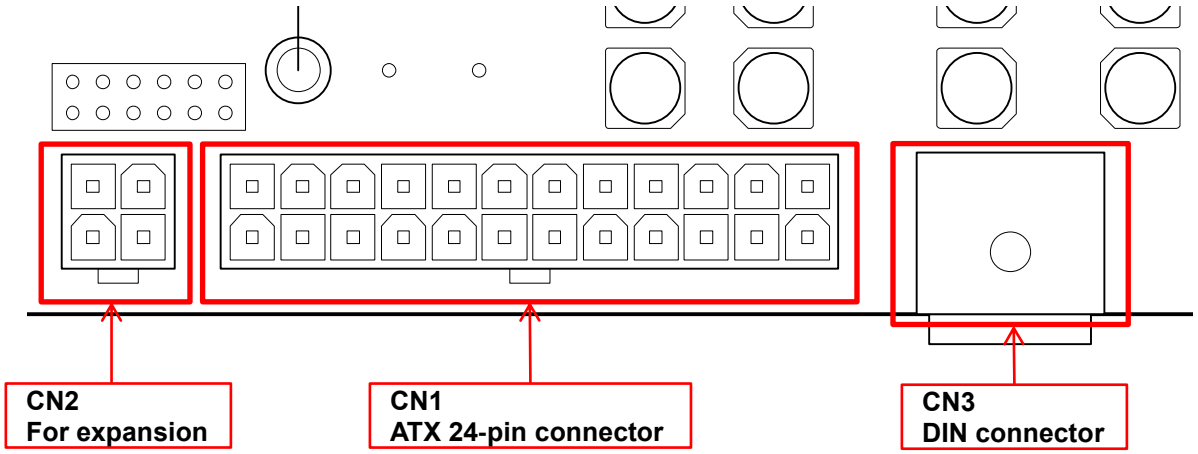

Figure 7.1.1-1 Power Input Connectors

⚠ **Warning**	If you plug an AC adapter other than the one provided with the product into CN3, and then use the board, you may damage or break the board, depending on the specifications of the output terminal of that power supply. Always use the AC adapter provided. The CN1 and CN2 ATX power supply connectors are not guaranteed to connect to all ATX power supplies.

7.1.2.Power Switch

Use SW1, shown in the following diagram, to turn the board's power supply on and off.
Sliding the SW1 switch to the ON side turns on the power to the board.

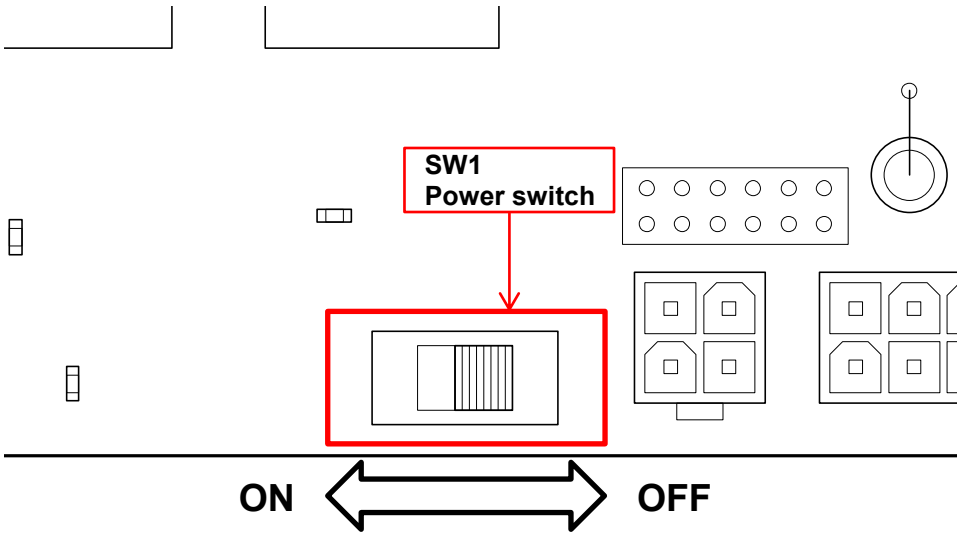

Figure 7.1.2-1 Power Switch

7.1.3.Power Supply Control IC

The board is equipped with an LT2977 (U3) power supply control IC manufactured by Linear Technology. You can monitor the voltage and control the power supply ICs by connecting the DC1613A PMBus controller for the Linear Technology LTpowerPlay to CN4.
* Confirm the details about how to use the LT2977 and the DC1613A in the respective data sheets.

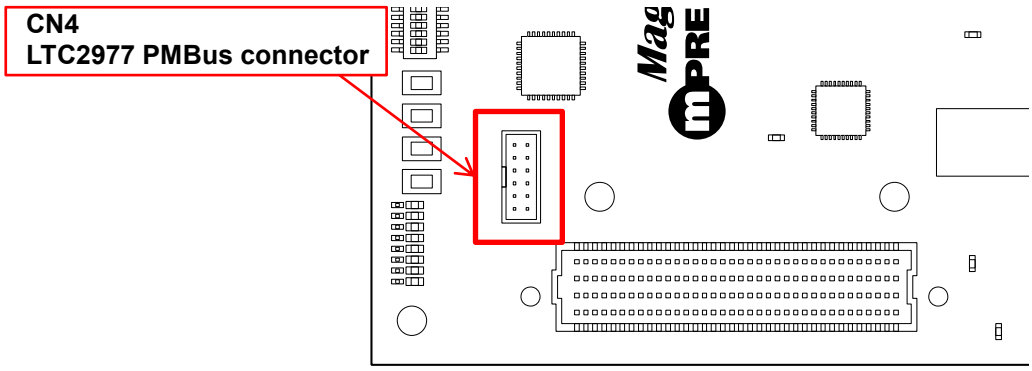

Figure 7.1.3-1 DC1613A Connection

The U3 pins and power supply ICs, and the monitored voltage connections are shown below.
* Be careful, because the VOUT_ENx and VSENSEPx do not all have 1 to 1 relationships.

Table 7.1.3-1 U3 VOUT_EN

U3 Pin Name	Signal Name	Reference	Model number	Voltage name
VOUT_EN0	PW_EN1	U4	EM2140P01QI	FP+0p95v
VOUT_EN1	PW_EN2	U6	EM2120L01QI	GXB+1p03v
VOUT_EN2	PW_EN3	U7	EM2120H01QI	BD+5v
VOUT_EN3	PW_EN4	U8	EN6362QI	FP_1p8v-1,FP_VCCAPLL+1p8v
VOUT_EN4	PW_EN5	U9	EN6382QI	FP+1p8v-2
		U10	EN6362QI	FP+1p8v-3
		U11	LTM4632EV#PBF	FP_DDR4+1p2v,DDR4_VTT+0p6v, DDR4_VREF+0p6v
		U12	EN6310QI	DDR4+2p5v
		U13	EM2120H01QI	BD+3p3v
VOUT_EN5	PW_EN6	U5	ER3110DI	EM21+5v
VOUT_EN6	-	-	-	-
VOUT_EN7	-	-	-	-

Table 7.1.3-2 U3 VSENSEP

U3 Pin Name	Monitored voltage
VSENSEP0	FP+0p95v
VSENSEP1	GXB+1p03v
VSENSEP2	BD+5v
VSENSEP3	FP+1p8v-1
VSENSEP4	FP+1p8v-2
VSENSEP5	FP+1p8v-3
VSENSEP6	FP_DDR4+1p2v
VSENSEP7	BD+3p3v

7.1.4.Power Status LED

You can check the power supply on the board by which of the 11 LEDs mounted on the board are lit.

Table 7.1.4-1 Power Status LED

Power	Reference	Locations of main uses	Color
EM21+5v	LED12	EM21xx Power supply IC (U4, U6, U7, U13) PVCC	Green
FP+0p95V	LED13	FPGA VCC/VCCP/VCCBRAM	Green
GXB+1p03v	LED14	FPGA VCCR_GXB/VCCT_GXB	Green
BD+5v	LED15	Various DC/DC, SATA, USB	Green
FP+1p8v-1	LED16	FPGA VCCPT/VCCBAT/VCCAPLL/ VCCH_GXB	Green
FP+1p8v-2	LED17	FPGA VCCIO(2K/2L/3G/3H), FMC(HPC) Vadj	Green
FP+1p8v-3	LED18	FPGAVCCIO(2A/2I/2J/3A/3B)/VCCPGM, FMC(LPC) Vadj,Si5341	Green
FP_DDR4+1p2v	LED19	FPGA VCCIO(3C/3D/2L/2K),DDR4 SDRAM	Green
DDR4+2p5v	LED20	DDR4 SDRAM VPP	Green
DDR4_VTT+0p6v	LED21	DDR4 Vref/Termination	Green
BD+3p3v	LED22	FMC AUX,SATA, COMe/FPGA Peripherals	Green

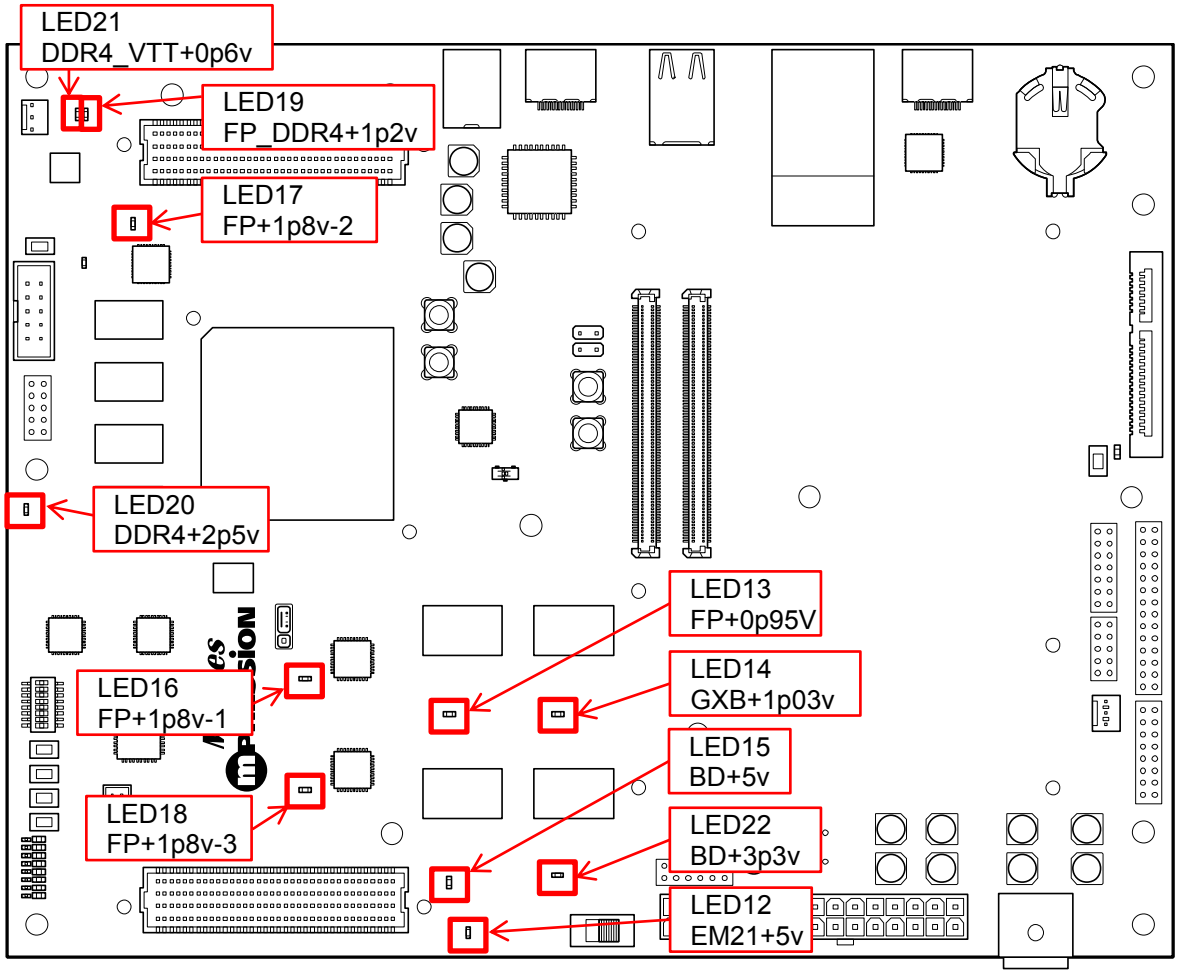

Figure 7.1.4-1 Power Status LED

7.2. FPGA

The board is equipped with an Arria10 GX FPGA (10AX090N2F40E2SG) manufactured by Intel.
The following describes the functions that can be evaluated on the FPGA with the board.

- DDR4-SDRAM
- HDMI image output connector (Type-A)
- FMC connector (HPC x1 and LPC x1)
- USB connector (Type-B) for USB UART
- IF (DIP switches, push switches, LEDs) for various debugging
- COM Express (PCI Express Gen2x4Lane)

7.2.1.FPGA Configuration Components

The board is equipped with a JTAG connector (CN5) for FPGA configuration and an Intel EPCQL1024F24IN (U15) as the ROM for FPGA configuration.
ROM configuration mode AS is supported, and Fast or Standard can be selected for the Power-On Reset (POR) Delay depending on how the JP5 jumper socket is installed.
LED 1 lights when the FPGA configuration is complete.
You can also reconfigure the FPGA by pressing SW8.

A block diagram of the FPGA configuration components is shown below.

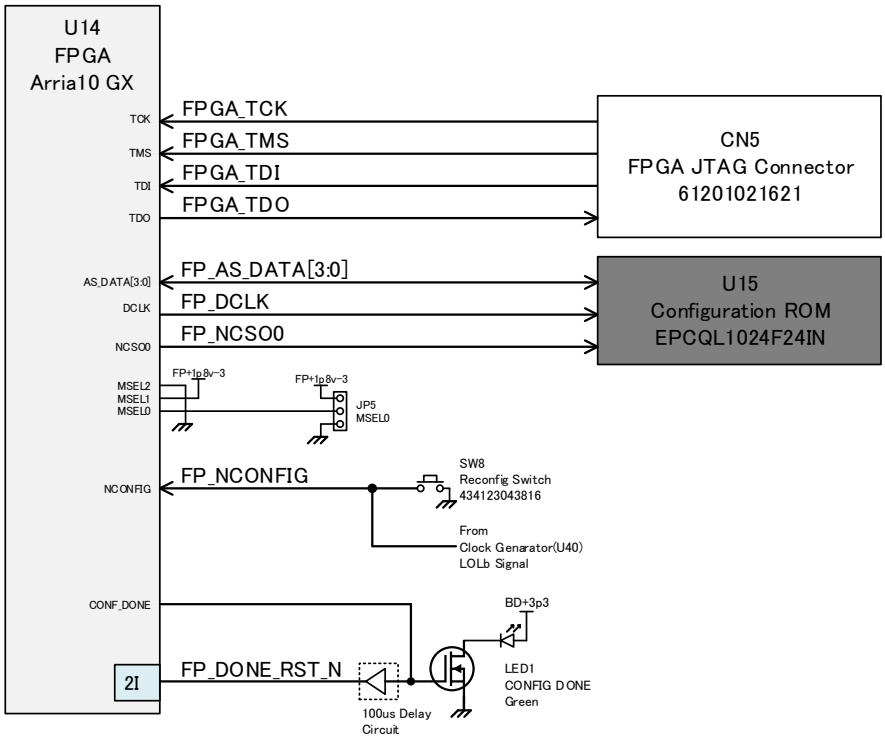

Figure 7.2.1-1 FPGA Configuration Components Block Diagram

7.2.1.1. FPGA JTAG Connector

The board is equipped with a JTAG connector (CN5) for connecting the Intel® FPGA Download Cable II.
To connect to a PC, connect the Intel FPGA Download Cable II to the JTAG connector as shown in the figure below.

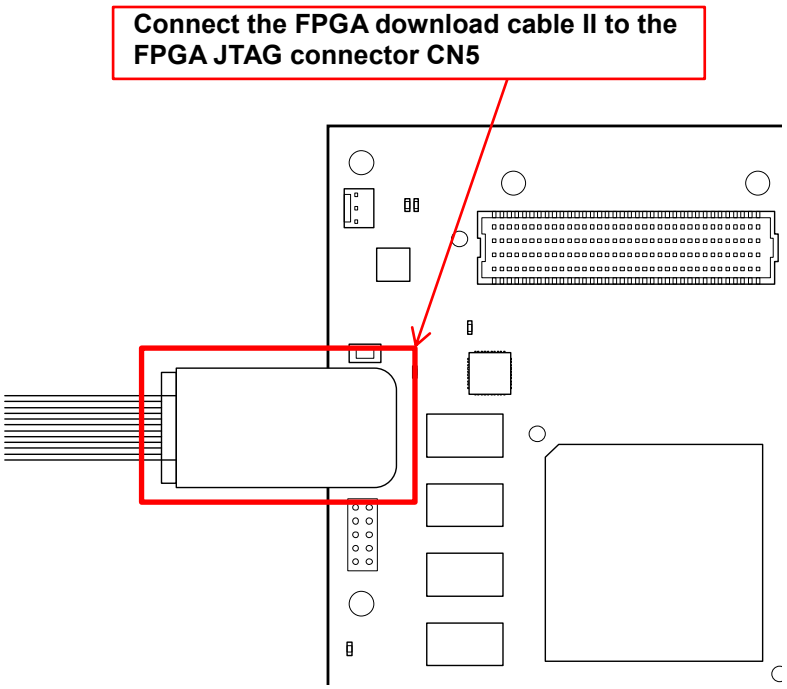

Figure 7.2.1-2 CN5 (FPGA JTAG) Connector

7.2.1.2. Switching the Power-On Reset Delay

You can set the setting of the MSEL on the FPGA to 011 or 010 by using the settings of the JP5 jumper socket so it is possible to set the Power-On Reset (POR) Delay to standard or fast.

Table 7.2.1-1 JP5 Settings

Position to attach the jumper socket	MSEL[2:0]	POR Delay
1-2	011	Standard
2-3	010	Fast

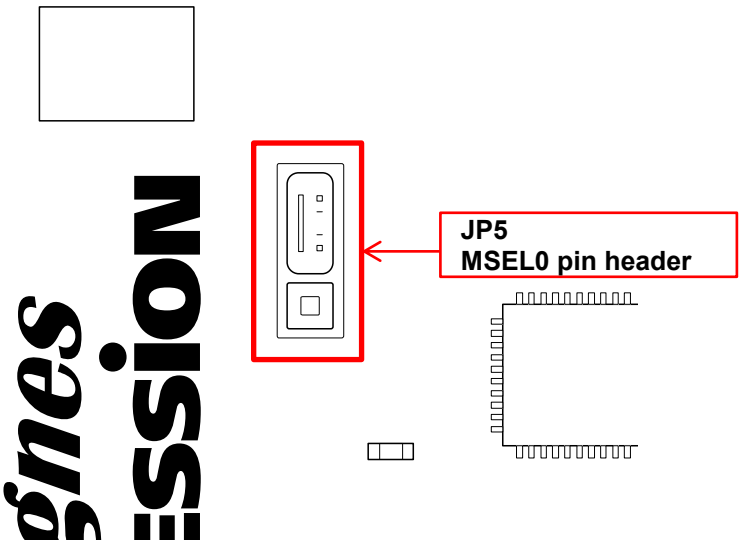

Figure 7.2.1-3 JP5 (MSEL0) Mount Diagram

7.2.1.3. Configuration Done LED

The board is equipped with an LED (LED1) to indicate that the configuration of the FPGA is complete, so you can confirm that configuration of the FPGA has been completed successfully. This LED lights when the configuration is complete.
It does not light while the FPGA is being configured or if the configuration does not finish successfully.

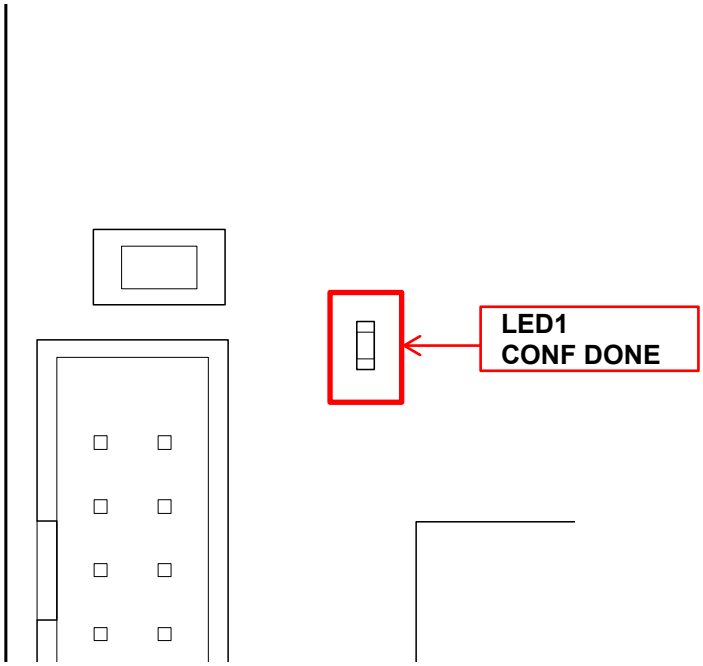

Figure 7.2.1-4 LED1 (CONF DONE)

7.2.1.4. Reconfiguration Switch

The board is equipped with a switch (SW8) to reconfigure the FPGA.
Pressing SW8 starts reconfiguration of the FPGA.

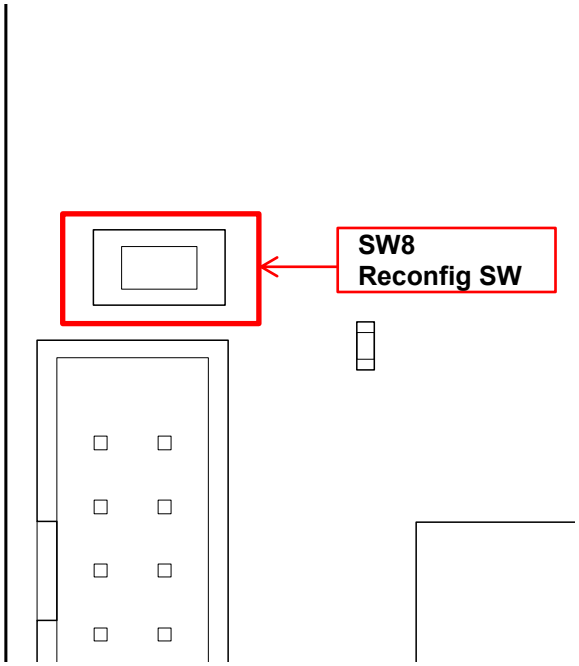

Figure 7.2.1-5 SW8 (Reconfiguration Switch)

7.2.2.Clock Generator/SMA Connector

The board is equipped with 3 (U39, U40, and U41) Silicon Laboratory Si5340B clock generators as clock sources for the FPGA.
Each of the clock ICs is set with individual output frequencies, so the individual clock ICs do not need to be set from the outside. However, it is possible to change the settings from the FPGA, COMe module, or JP6 by using the I2C.
Each of the clock ICs outputs a clock that is set so that the resonator connected to each clock IC is set to the master as a reference clock. Note that for U41, you can select a resonator or oscillator for the master of the reference clock by setting SW7.

The board is also equipped with 4 SMA connectors (1 pair each for input/output) for input/output of differential clocks so CN17 and CN18 can supply differential clock to the outside through OUT3 of U41.
You can supply differential clock to the FPGA from the outside by using CN19 and CN20. Note that the input/output part of the SMA connector is AC coupled.

Caution	To supply differential clock to the FPGA from the outside, you need to confirm the AC parameters and DC parameters of the FPGA and be careful to comply with the input ratings of the FPGA.

A block diagram of the clock generator/SMA connector and FPGA peripherals is shown below.

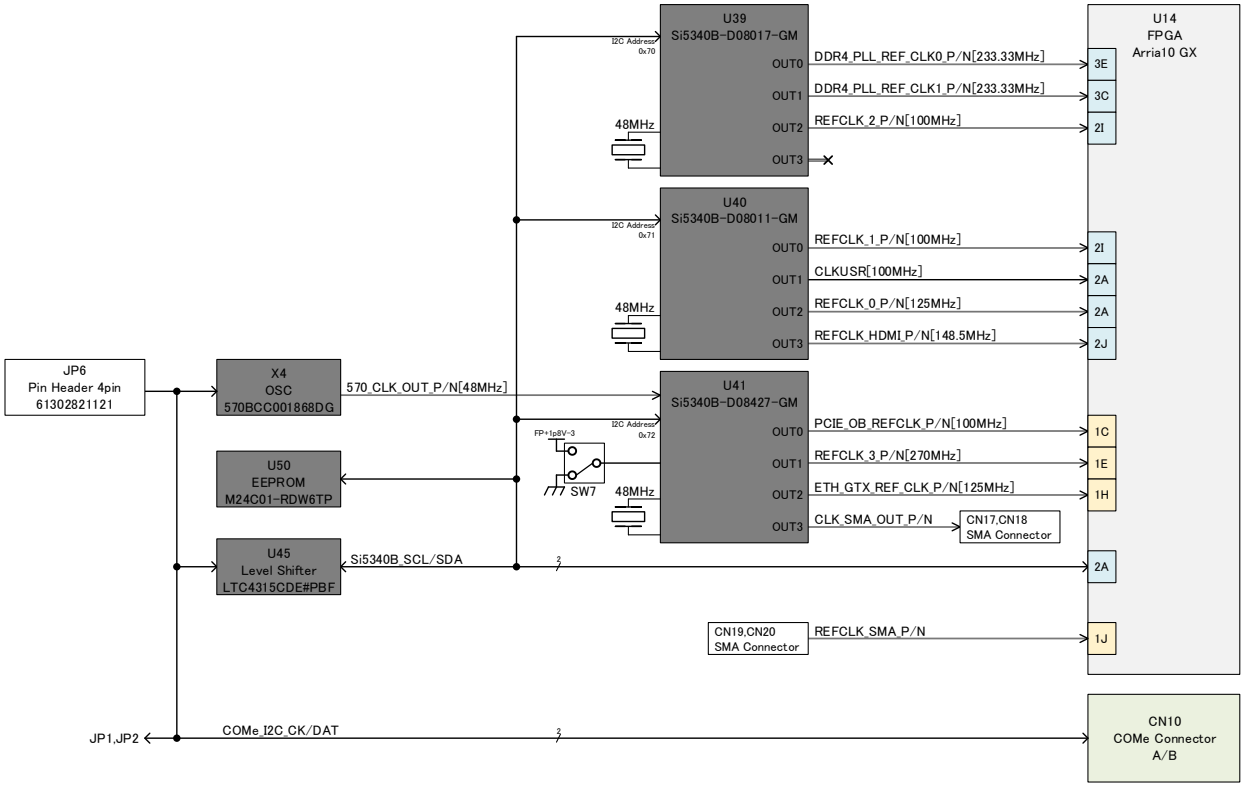

Figure 7.2.2-1 FPGA Clock Generator/SMA Connector Block Diagram

Table 7.2.2-1 Clock Generator Output

Reference	Output	Frequency	Signal Name	FPGA	
				Pin No	Bank
U39	OUT0	233.33 MHz	DDR4_PLL_REF_CLK0_P	W5	3E
	OUT0b		DDR4_PLL_REF_CLK0_N	W6	3E
	OUT1	233.33 MHz	DDR4_PLL_REF_CLK1_P	AG5	3C
	OUT1b		DDR4_PLL_REF_CLK1_N	AG6	3C
	OUT2	100 MHz	REFCLK_2_P	AM21	2I
	OUT2b		REFCLK_2_N	AL20	2I
	OUT3	-	-	-	-
	OUT3b		-	-	-
U40	OUT0	100 MHz	REFCLK_1_P	AJ21	2I
	OUT0b		REFCLK_1_N	AH21	2I
	OUT1	100 MHz	CLKUSR	AP20	2A
	OUT1b		-	-	-
	OUT2	125 MHz	REFCLK_0_P	AT18	2A
	OUT2b		REFCLK_0_N	AR18	2A
	OUT3	148.5 MHz	REFCLK_HDMI_P	AP26	2J
	OUT3b		REFCLK_HDMI_N	AN26	2J
U41	OUT0	100 MHz	PCIE_OB_REFCLK_P	AN29	1C
	OUT0b		PCIE_OB_REFCLK_N	AN28	1C
	OUT1	270 MHz	REFCLK_3_P	AE29	1E
	OUT1b		REFCLK_3_N	AE28	1E
	OUT2	125 MHz	ETH_GTX_REF_CLK_P	R29	1H
	OUT2b		ETH_GTX_REF_CLK_N	R28	1H
	OUT3	270 MHz	CLK_SMA_OUT_P	* To CN17	
	OUT3b		CLK_SMA_OUT_N	* To CN18	

Table 7.2.2-2 SMA Connector Input

Reference	Signal Name	FPGA	
		Pin No	Bank
CN19	REFCLK_SMA_P	G29	1J
CN20	REFCLK_SMA_N	G28	1J

7.2.2.1. U41 Reference Clock Switch

On U41, you can switch the setting for the IN_SEL terminal of U41 by switching SW7. This makes it possible to switch the reference clock's master to resonator (X5) or oscillator (X4).

Table 7.2.2-3 U41 Reference Clock Switch

SW7	Reference	Model number	Manufacturer
1-2	X5	C7L-48000-080-BQ4-J7	River Eletec
2-3	X4	570BCC001868DG	Silicon Labs

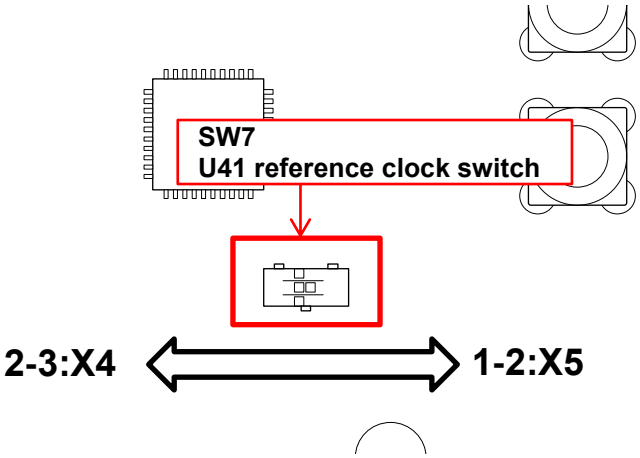

Figure 7.2.2-2 Clock Switch SW7

7.2.2.2. SMA Connector

The board is equipped with 2 pairs of SMA connectors, 1 each for input/output of clocks, for a total of 4.
The output connector is connected to the OUT3 of U41, and the input connector is connected to 1J Bank on the FPGA.
For details refer to Table 8.2-2 and Table 8.2-3.

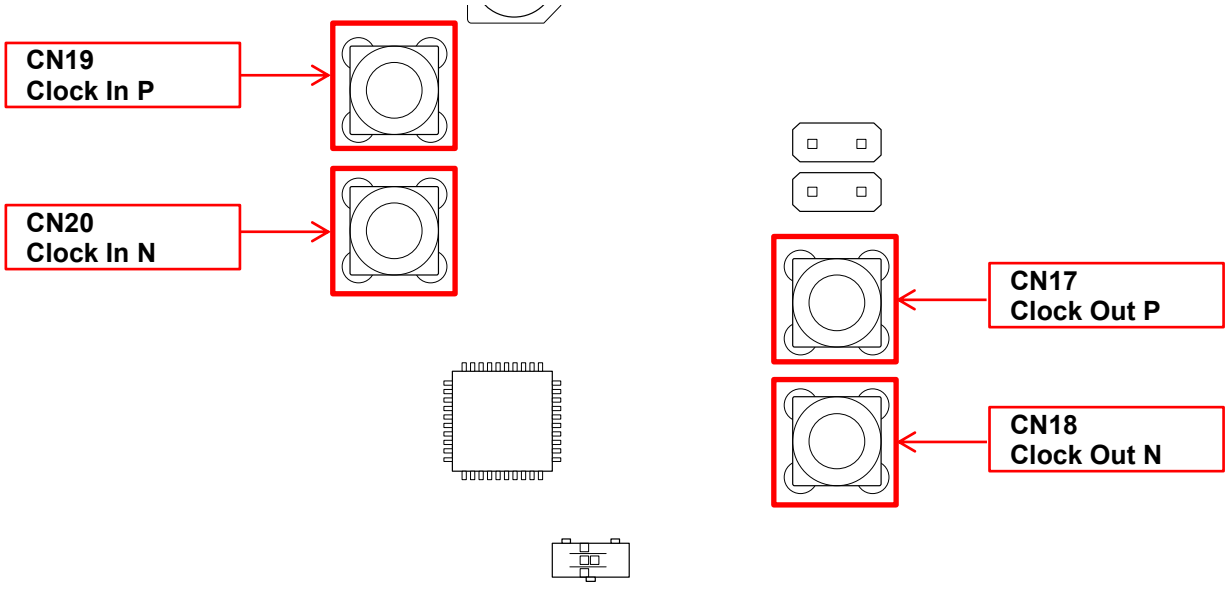

Figure 7.2.2-3 SMA Connectors

7.2.2.3. I2C Connectors for Clocks

The board is equipped with a pin header (JP6) that can be connected to the I2C bus, which is connected to the FPGA, COMe module, clock generator, oscillator, and EEPROM.

Table 7.2.2-4 JP6 Pin Assignment

JP6 Pin No	Signal Name
1	BD+3p3v
2	570B_SDA
3	570B_SCL
4	GND

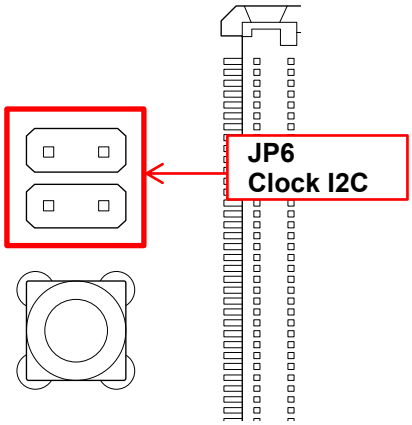

Figure 7.2.2-4 JP6

7.2.3.DDR4 SDRAM

The board is equipped with 4 DDR4 SDRAM (MT40A512M16JY-083E) manufactured by Micron.
The address, command, and clock signals are wired in a fly-by topology.

- Specifications
  8 Gbit (64M word x 16 bit x 8 banks) x 4
  * 32 bit (16 bit x 2) x 2 systems
  * Board wiring is optimized for DDR4-1866 (933 MHz)

- Address configuration
  Address: 16 bit (Row address: 16 bit/Column address: 10 bit)
  Bank address: 2 bit
  Bank group address: 1 bit

- Data bus configuration
  Data strobe (DQS) of writing and reading is controlled in byte units
  Data mask (DM) is controlled in byte units

A block diagram of the area around the FPGA and DDR4 SDRAM is shown below.

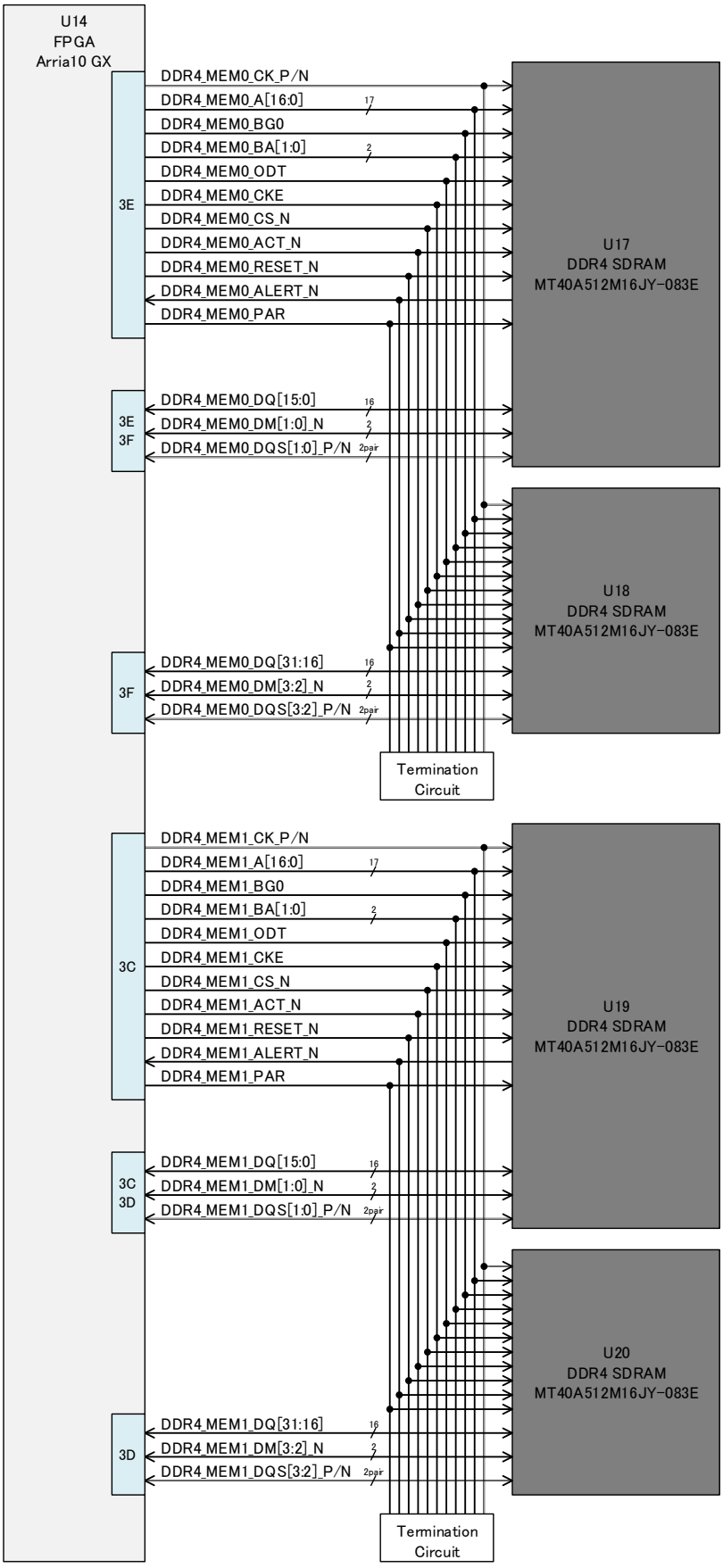

Figure 7.2.3-1 FPGA-DDR4 SDRAM Block Diagram

7.2.3.1. FPGA-DDR4 SDRAM Pin Assignment Table

The following table shows the pin assignments of the FPGA and DDR4 SDRAM on the board.

Table 7.2.3-1 FPGA-DDR4 SDRAM (U17) Pin Assignment

U17 Pin Name	Signal Name	FPGA		U17 Pin Name	Signal Name	FPGA	
		Pin No.	Bank			Pin No.	Bank
P3	DDR4_MEM0_A0	V3	3E	G2	DDR4_MEM0_DQ0	P4	3E
P7	DDR4_MEM0_A1	V4	3E	F7	DDR4_MEM0_DQ1	P1	3E
R3	DDR4_MEM0_A2	W3	3E	H3	DDR4_MEM0_DQ2	R1	3E
N7	DDR4_MEM0_A3	W4	3E	H7	DDR4_MEM0_DQ3	R2	3E
N3	DDR4_MEM0_A4	V1	3E	H2	DDR4_MEM0_DQ4	R3	3E
P8	DDR4_MEM0_A5	V2	3E	H8	DDR4_MEM0_DQ5	N3	3E
P2	DDR4_MEM0_A6	U1	3E	J3	DDR4_MEM0_DQ6	N4	3E
R8	DDR4_MEM0_A7	U2	3E	J7	DDR4_MEM0_DQ7	M1	3E
R2	DDR4_MEM0_A8	T2	3E	A3	DDR4_MEM0_DQ8	L9	3F
R7	DDR4_MEM0_A9	T3	3E	B8	DDR4_MEM0_DQ9	P11	3F
M3	DDR4_MEM0_A10	U4	3E	C3	DDR4_MEM0_DQ10	R11	3F
T2	DDR4_MEM0_A11	T4	3E	C7	DDR4_MEM0_DQ11	P9	3F
M7	DDR4_MEM0_A12	V7	3E	C2	DDR4_MEM0_DQ12	R10	3F
T8	DDR4_MEM0_A13	U5	3E	C8	DDR4_MEM0_DQ13	N8	3F
L2	DDR4_MEM0_A14	U6	3E	D3	DDR4_MEM0_DQ14	M9	3F
M8	DDR4_MEM0_A15	T7	3E	D7	DDR4_MEM0_DQ15	N9	3F
L8	DDR4_MEM0_A16	U7	3E	E7	DDR4_MEM0_DM0_N	M2	3E
N2	DDR4_MEM0_BA0	T5	3E	E2	DDR4_MEM0_DM1_N	P10	3F
N8	DDR4_MEM0_BA1	P5	3E	G3	DDR4_MEM0_DQS0_P	N1	3E
M2	DDR4_MEM0_BG0	P6	3E	F3	DDR4_MEM0_DQS0_N	N2	3E
K3	DDR4_MEM0_ODT	W9	3E	B7	DDR4_MEM0_DQS1_P	P8	3F
K2	DDR4_MEM0_CKE	T8	3E	A7	DDR4_MEM0_DQS1_N	R8	3F
L7	DDR4_MEM0_CS_N	U11	3E	K7	DDR4_MEM0_CK_P	V8	3E
L3	DDR4_MEM0_ACT_N	V11	3E	K8	DDR4_MEM0_CK_N	V9	3E
P1	DDR4_MEM0_RESET_N	R7	3E	A1 etc.	FP_DDR4+1p2v	-	-
GND	-	-	3E	B3 etc.	FP_DDR4+1p2v	-	-
P9	DDR4_MEM0_ALERT_N	P3	3E	B1,R9	DDR4+2p5v	-	-
T3	DDR4_MEM0_PAR	U10	3E	M1	DDR4_VREF+0p6v	-	-

Table 7.2.3-2 FPGA-DDR4 SDRAM (U18) Pin Assignment

U18 Pin Name	Signal Name	FPGA		U18 Pin Name	Signal Name	FPGA	
		Pin No.	Bank			Pin No.	Bank
P3	DDR4_MEM0_A0	V3	3E	G2	DDR4_MEM0_DQ16	M5	3F
P7	DDR4_MEM0_A1	V4	3E	F7	DDR4_MEM0_DQ17	L4	3F
R3	DDR4_MEM0_A2	W3	3E	H3	DDR4_MEM0_DQ18	M4	3F
N7	DDR4_MEM0_A3	W4	3E	H7	DDR4_MEM0_DQ19	K7	3F
N3	DDR4_MEM0_A4	V1	3E	H2	DDR4_MEM0_DQ20	L7	3F
P8	DDR4_MEM0_A5	V2	3E	H8	DDR4_MEM0_DQ21	K5	3F
P2	DDR4_MEM0_A6	U1	3E	J3	DDR4_MEM0_DQ22	K6	3F
R8	DDR4_MEM0_A7	U2	3E	J7	DDR4_MEM0_DQ23	N6	3F
R2	DDR4_MEM0_A8	T2	3E	A3	DDR4_MEM0_DQ24	K3	3F
R7	DDR4_MEM0_A9	T3	3E	B8	DDR4_MEM0_DQ25	L2	3F
M3	DDR4_MEM0_A10	U4	3E	C3	DDR4_MEM0_DQ26	L3	3F
T2	DDR4_MEM0_A11	T4	3E	C7	DDR4_MEM0_DQ27	H3	3F

U18 Pin Name	Signal Name	FPGA		U18 Pin Name	Signal Name	FPGA	
		Pin No.	Bank			Pin No.	Bank
M7	DDR4_MEM0_A12	V7	3E	C2	DDR4_MEM0_DQ28	H4	3F
T8	DDR4_MEM0_A13	U5	3E	C8	DDR4_MEM0_DQ29	H1	3F
L2	DDR4_MEM0_A14	U6	3E	D3	DDR4_MEM0_DQ30	J1	3F
M8	DDR4_MEM0_A15	T7	3E	D7	DDR4_MEM0_DQ31	J4	3F
L8	DDR4_MEM0_A16	U7	3E	E7	DDR4_MEM0_DM2_N	N7	3F
N2	DDR4_MEM0_BA0	T5	3E	E2	DDR4_MEM0_DM3_N	K2	3F
N8	DDR4_MEM0_BA1	P5	3E	G3	DDR4_MEM0_DQS2_P	M6	3F
M2	DDR4_MEM0_BG0	P6	3E	F3	DDR4_MEM0_DQS2_N	M7	3F
K3	DDR4_MEM0_ODT	W9	3E	B7	DDR4_MEM0_DQS3_P	K1	3F
K2	DDR4_MEM0_CKE	T8	3E	A7	DDR4_MEM0_DQS3_N	K2	3F
L7	DDR4_MEM0_CS_N	U11	3E	K7	DDR4_MEM0_CK_P	V8	3E
L3	DDR4_MEM0_ACT_N	V11	3E	K8	DDR4_MEM0_CK_N	V9	3E
P1	DDR4_MEM0_RESET_N	R7	3E	A1 etc.	FP_DDR4+1p2v	-	-
GND	-	-	3E	B3 etc.	FP_DDR4+1p2v	-	-
P9	DDR4_MEM0_ALERT_N	P3	3E	B1,R9	DDR4+2p5v	-	-
T3	DDR4_MEM0_PAR	U10	3E	M1	DDR4_VREF+0p6v	-	-

Table 7.2.3-3 FPGA-DDR4 SDRAM (U19) Pin Assignment

U19 Pin Name	Signal Name	FPGA		U19 Pin Name	Signal Name	FPGA	
		Pin No.	Bank			Pin No.	Bank
P3	DDR4_MEM1_A0	AN3	3C	G2	DDR4_MEM1_DQ0	AF10	3C
P7	DDR4_MEM1_A1	AM4	3C	F7	DDR4_MEM1_DQ1	AD10	3C
R3	DDR4_MEM1_A2	AL3	3C	H3	DDR4_MEM1_DQ2	AC11	3C
N7	DDR4_MEM1_A3	AL4	3C	H7	DDR4_MEM1_DQ3	AD8	3C
N3	DDR4_MEM1_A4	AL5	3C	H2	DDR4_MEM1_DQ4	AD9	3C
P8	DDR4_MEM1_A5	AK5	3C	H8	DDR4_MEM1_DQ5	AE10	3C
P2	DDR4_MEM1_A6	AK6	3C	J3	DDR4_MEM1_DQ6	AE11	3C
R8	DDR4_MEM1_A7	AJ6	3C	J7	DDR4_MEM1_DQ7	AC8	3C
R2	DDR4_MEM1_A8	AK3	3C	A3	DDR4_MEM1_DQ8	AE3	3D
R7	DDR4_MEM1_A9	AJ4	3C	B8	DDR4_MEM1_DQ9	AE1	3D
M3	DDR4_MEM1_A10	AJ5	3C	C3	DDR4_MEM1_DQ10	AE2	3D
T2	DDR4_MEM1_A11	AH6	3C	C7	DDR4_MEM1_DQ11	AG2	3D
M7	DDR4_MEM1_A12	AG7	3C	C2	DDR4_MEM1_DQ12	AF2	3D
T8	DDR4_MEM1_A13	AJ3	3C	C8	DDR4_MEM1_DQ13	AC2	3D
L2	DDR4_MEM1_A14	AH3	3C	D3	DDR4_MEM1_DQ14	AD3	3D
M8	DDR4_MEM1_A15	AF7	3C	D7	DDR4_MEM1_DQ15	AD1	3D
L8	DDR4_MEM1_A16	AE7	3C	E7	DDR4_MEM1_DM0_N	AC9	3C
N2	DDR4_MEM1_BA0	AF5	3C	E2	DDR4_MEM1_DM1_N	AC1	3D
N8	DDR4_MEM1_BA1	AH4	3C	G3	DDR4_MEM1_DQS0_P	AF8	3C
M2	DDR4_MEM1_BG0	AG4	3C	F3	DDR4_MEM1_DQS0_N	AE8	3C
K3	DDR4_MEM1_ODT	AR1	3C	B7	DDR4_MEM1_DQS1_P	AH1	3D
K2	DDR4_MEM1_CKE	AM1	3C	A7	DDR4_MEM1_DQS1_N	AG1	3D
L7	DDR4_MEM1_CS_N	AM2	3C	K7	DDR4_MEM1_CK_P	AK1	3C
L3	DDR4_MEM1_ACT_N	AL2	3C	K8	DDR4_MEM1_CK_N	AK2	3C
P1	DDR4_MEM1_RESET_N	AN2	3C	A1 etc.	FP_DDR4+1p2v	-	-
GND	-	-	-	B3 etc.	FP_DDR4+1p2v	-	-
P9	DDR4_MEM1_ALERT_N	AF9	3C	B1,R9	DDR4+2p5v	-	-
T3	DDR4_MEM1_PAR	AH2	3C	M1	DDR4_VREF+0p6v	-	-

Table 7.2.3-4 FPGA-DDR4 SDRAM (U20) Pin Assignment

U20 Pin Name	Signal Name	FPGA		U20 Pin Name	Signal Name	FPGA	
		Pin No.	Bank			Pin No.	Bank
P3	DDR4_MEM1_A0	AN3	3C	G2	DDR4_MEM1_DQ16	AC4	3D
P7	DDR4_MEM1_A1	AM4	3C	F7	DDR4_MEM1_DQ17	AB1	3D
R3	DDR4_MEM1_A2	AL3	3C	H3	DDR4_MEM1_DQ18	AB2	3D
N7	DDR4_MEM1_A3	AL4	3C	H7	DDR4_MEM1_DQ19	AB4	3D
N3	DDR4_MEM1_A4	AL5	3C	H2	DDR4_MEM1_DQ20	AA4	3D
P8	DDR4_MEM1_A5	AK5	3C	H8	DDR4_MEM1_DQ21	Y1	3D
P2	DDR4_MEM1_A6	AK6	3C	J3	DDR4_MEM1_DQ22	W1	3D
R8	DDR4_MEM1_A7	AJ6	3C	J7	DDR4_MEM1_DQ23	Y2	3D
R2	DDR4_MEM1_A8	AK3	3C	A3	DDR4_MEM1_DQ24	AB6	3D
R7	DDR4_MEM1_A9	AJ4	3C	B8	DDR4_MEM1_DQ25	AD6	3D
M3	DDR4_MEM1_A10	AJ5	3C	C3	DDR4_MEM1_DQ26	AC6	3D
T2	DDR4_MEM1_A11	AH6	3C	C7	DDR4_MEM1_DQ27	AD4	3D
M7	DDR4_MEM1_A12	AG7	3C	C2	DDR4_MEM1_DQ28	AD5	3D
T8	DDR4_MEM1_A13	AJ3	3C	C8	DDR4_MEM1_DQ29	AA5	3D
L2	DDR4_MEM1_A14	AH3	3C	D3	DDR4_MEM1_DQ30	Y5	3D
M8	DDR4_MEM1_A15	AF7	3C	D7	DDR4_MEM1_DQ31	Y6	3D
L8	DDR4_MEM1_A16	AE7	3C	E7	DDR4_MEM1_DM2_N	Y3	3D
N2	DDR4_MEM1_BA0	AF5	3C	E2	DDR4_MEM1_DM3_N	Y7	3D
N8	DDR4_MEM1_BA1	AH4	3C	G3	DDR4_MEM1_DQS2_P	AA2	3D
M2	DDR4_MEM1_BG0	AG4	3C	F3	DDR4_MEM1_DQS2_N	AA3	3D
K3	DDR4_MEM1_ODT	AR1	3C	B7	DDR4_MEM1_DQS3_P	AE5	3D
K2	DDR4_MEM1_CKE	AM1	3C	A7	DDR4_MEM1_DQS3_N	AE6	3D
L7	DDR4_MEM1_CS_N	AM2	3C	K7	DDR4_MEM1_CK_P	AK1	3C
L3	DDR4_MEM1_ACT_N	AL2	3C	K8	DDR4_MEM1_CK_N	AK2	3C
P1	DDR4_MEM1_RESET_N	AN2	3C	A1 etc.	FP_DDR4+1p2v	-	-
GND	-	-	-	B3 etc.	FP_DDR4+1p2v	-	-
P9	DDR4_MEM1_ALERT_N	AF9	3C	B1,R9	DDR4+2p5v	-	-
T3	DDR4_MEM1_PAR	AH2	3C	M1	DDR4_VREF+0p6v	-	-

7.2.4.FPGA-HDMI Output

The board is equipped with an ADV7511KSTZ-P (U21) manufactured by Analog Devices, for HDMI output from the FPGA. The connector for HDMI output is an HDMI Type-A (CN6).
The data bus that is connected to the FPGA is 24 bit (8 bit x 3). Refer to the specification sheet of the ADV7511K for the supported video formats.

Caution	This HDMI output interface does not support audio output. Furthermore, the board is equipped with an HDMI output connector (CN14) for the COMe module, which is the same shape connector, so be careful when connecting to it.

A block diagram of the area around the FPGA and HDMI output is shown below.

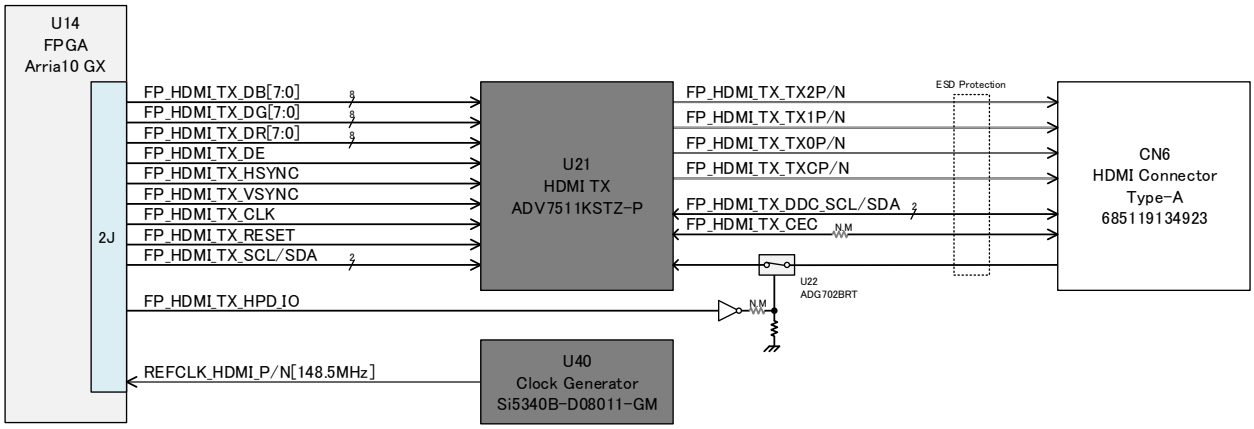

Figure 7.2.4-1 FPGA-HDMI Output Area Block Diagram

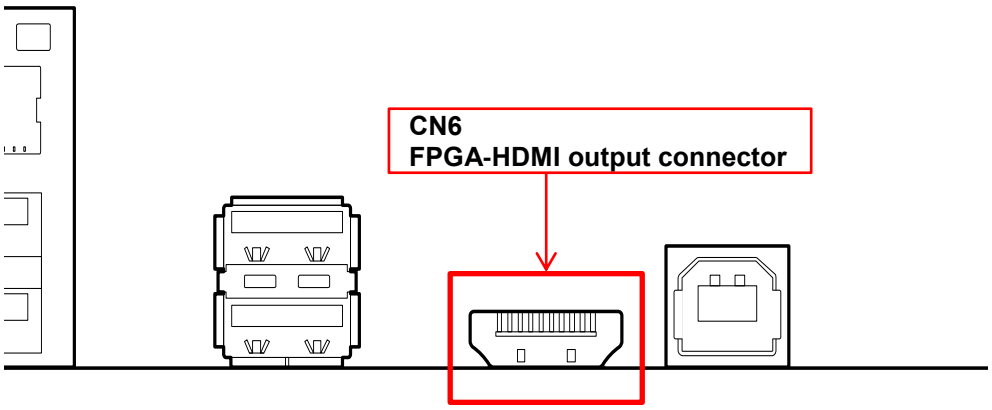

Figure 7.2.4-2 FPGA-HDMI Output Connector

7.2.4.1. HDMI I2C Address

U21 is controlled from the FPGA via the I2C bus. The slave address of I2C is 0x72.

7.2.4.2. FPGA-HDMI TX IC Pin Assignment Table

The following table shows the pin assignments of the FPGA and HDMI TX IC (U21) on the board.

Table 7.2.4-1 FPGA-HDMI TX Pin Assignment Table

HDMI TX(U21)		Signal Name	FPGA	
Pin No.	Pin Name		Pin No.	Bank
57	D35	FP_HDMI_TX_R7	AV23	2J
58	D34	FP_HDMI_TX_R6	AW23	2J
59	D33	FP_HDMI_TX_R5	AU25	2J
60	D32	FP_HDMI_TX_R4	AU26	2J
61	D31	FP_HDMI_TX_R3	AR26	2J
62	D30	FP_HDMI_TX_R2	AT26	2J
63	D29	FP_HDMI_TX_R1	AT23	2J
64	D28	FP_HDMI_TX_R0	AU24	2J
69	D23	FP_HDMI_TX_G7	AL25	2J
70	D22	FP_HDMI_TX_G6	AM25	2J
71	D21	FP_HDMI_TX_G5	AK23	2J
72	D20	FP_HDMI_TX_G4	AL23	2J
73	D19	FP_HDMI_TX_G3	AM24	2J
74	D18	FP_HDMI_TX_G2	AL24	2J
78	D17	FP_HDMI_TX_G1	AH25	2J
80	D16	FP_HDMI_TX_G0	AJ26	2J
85	D11	FP_HDMI_TX_B7	AH23	2J
86	D10	FP_HDMI_TX_B6	AH24	2J
87	D9	FP_HDMI_TX_B5	AJ23	2J
88	D8	FP_HDMI_TX_B4	AJ24	2J
89	D7	FP_HDMI_TX_B3	AJ25	2J
90	D6	FP_HDMI_TX_B2	AK25	2J
91	D5	FP_HDMI_TX_B1	AF25	2J
92	D4	FP_HDMI_TX_B0	AG25	2J
97	DE	FP_HDMI_TX_DE	AW24	2J
98	HSYNC	FP_HDMI_TX_HSYNC	AW26	2J
2	VSYNC	FP_HDMI_TX_VSYNC	AV24	2J
79	CLK	FP_HDMI_TX_CLK	AT25	2J
38	PD	HDMI_TX_RESET_N	AV28	2J
45	INT	HDMI_TX_INT	AV27	2J
55	SCL	FP_HDMI_TX_SCL	AW25	2J
56	SDA	FP_HDMI_TX_SDA	AW28	2J
30	HPD	HDMI_TX_HPD_IO	AV26	2J

7.2.5.FMC Connectors

The board is equipped with two ASP-134486-01 FMC connectors (CN7 and CN9) manufactured by Samtec, for external extensions. The FPGA signals connected to the FMC connectors have different specifications: high pin count and low pin count. So, be careful when you insert an FMC daughter card.

- CN7 = FMC high pin count (HPC) connection
  XCVR TX/RX channel : 10ch
  LVDS channel : 80ch

- CN9 = FMC low pin count (LPC) connection
  XCVR TX/RX channel : 1ch
  LVDS channel : 34ch

A block diagram of the area around the FPGA and FMC connectors is shown below.

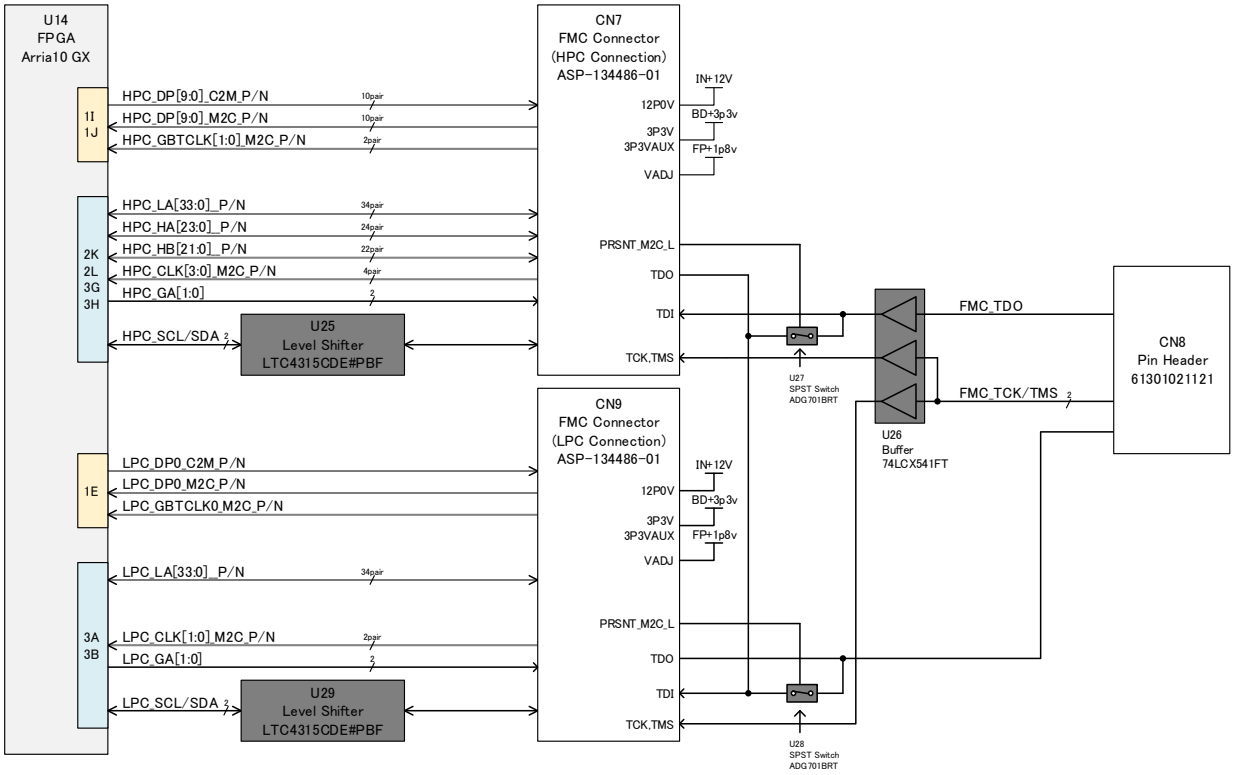

Figure 7.2.5-1 FPGA-FMC Output Area Block Diagram

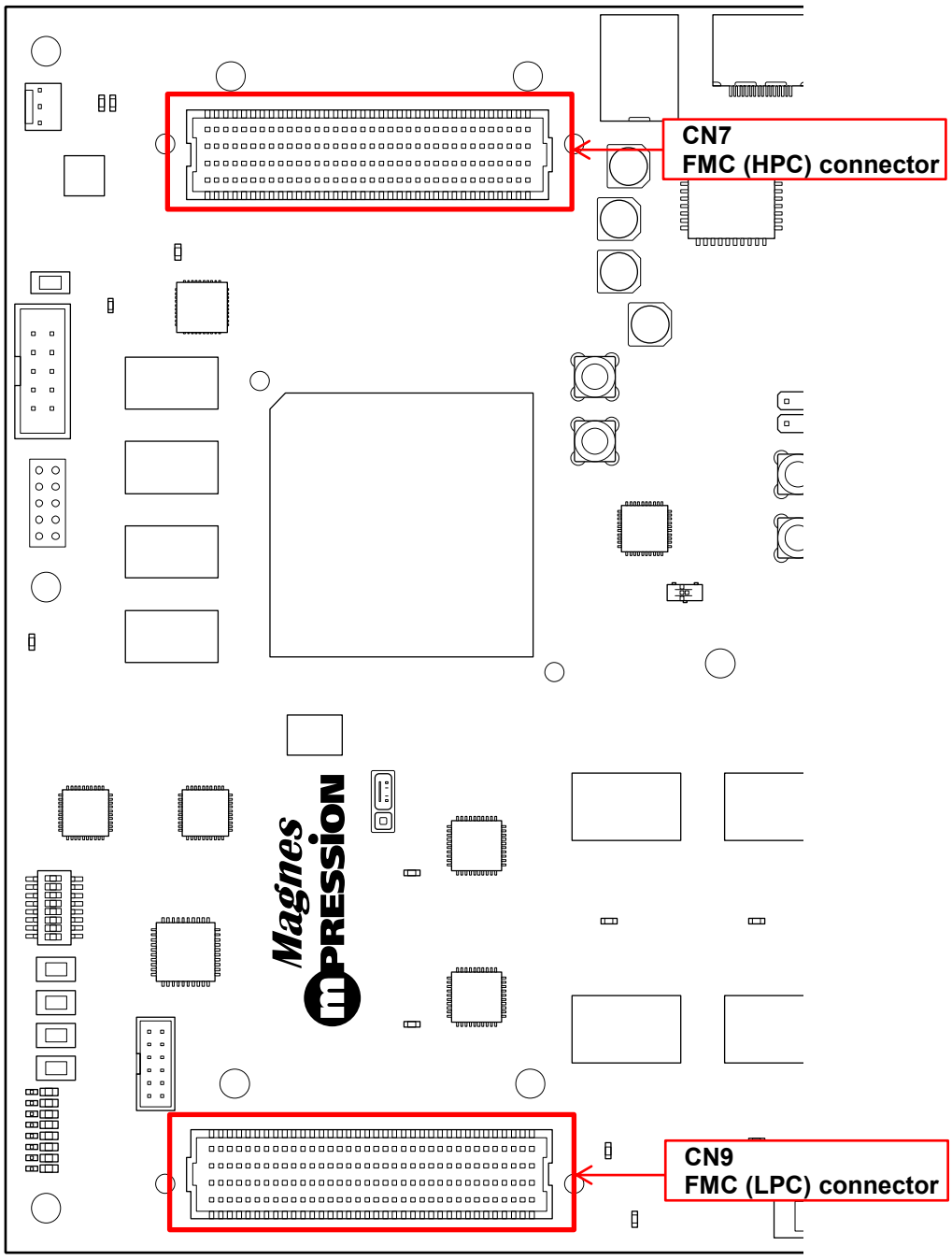

Figure 7.2.5-2 FMC Connector

7.2.5.1. FMC JTAG Connector (Not Mounted)

CN8 is the JTAG connector for FMC connectors.
You can access the JTAG line on the equipped FMC module through CN8.

Table 7.2.5-1 CN8 Pin Assignment

CN8 Pin No	Signal Name
1	FMC_TCK
2	GND
3	FMC_TDI
4	BD+3p3
5	FMC_TMS
6	-
7	-
8	-
9	FMC_TDO
10	GND

7.2.5.2. FMC Connector (HPC) Pin Assignment Table

The following table shows the pin assignments for the FPGA and CN7.

Table 7.2.5-2 FPGA-FMC Connector (CN7) Pin Assignment

CN7		Signal Name	FPGA	
Pin No	Pin Name		Pin No.	Bank
A1	GND	GND	-	-
A2	DP1_M2C_P	HPC_DP1_M2C_P	K31	1I
A3	DP1_M2C_N	HPC_DP1_M2C_N	K30	1I
A4	GND	GND	-	-
A5	GND	GND	-	-
A6	DP2_M2C_P	HPC_DP2_M2C_P	J33	1I
A7	DP2_M2C_N	HPC_DP2_M2C_N	J32	1I
A8	GND	GND	-	-
A9	GND	GND	-	-
A10	DP3_M2C_P	HPC_DP3_M2C_P	H35	1I
A11	DP3_M2C_N	HPC_DP3_M2C_N	H34	1I
A12	GND	GND	-	-
A13	GND	GND	-	-
A14	DP4_M2C_P	HPC_DP4_M2C_P	H31	1J
A15	DP4_M2C_N	HPC_DP4_M2C_N	H30	1J
A16	GND	GND	-	-
A17	GND	GND	-	-
A18	DP5_M2C_P	HPC_DP5_M2C_P	G33	1J
A19	DP5_M2C_N	HPC_DP5_M2C_N	G32	1J
A20	GND	GND	-	-
A21	GND	GND	-	-
A22	DP1_C2M_P	HPC_DP1_C2M_P	E37	1I
A23	DP1_C2M_N	HPC_DP1_C2M_N	E36	1I
A24	GND	GND	-	-
A25	GND	GND	-	-
A26	DP2_C2M_P	HPC_DP2_C2M_P	D39	1I
A27	DP2_C2M_N	HPC_DP2_C2M_N	D38	1I
A28	GND	GND	-	-
A29	GND	GND	-	-
A30	DP3_C2M_P	HPC_DP3_C2M_P	D35	1I
A31	DP3_C2M_N	HPC_DP3_C2M_N	D34	1I
A32	GND	GND	-	-
A33	GND	GND	-	-
A34	DP4_C2M_P	HPC_DP4_C2M_P	C37	1J
A35	DP4_C2M_N	HPC_DP4_C2M_N	C36	1J
A36	GND	GND	-	-
A37	GND	GND	-	-
A38	DP5_C2M_P	HPC_DP5_C2M_P	B39	1J
A39	DP5_C2M_N	HPC_DP5_C2M_N	B38	1J
A40	GND	GND	-	-
B1	RES1	GND	-	-
B2	GND	GND	-	-

CN7		Signal Name	FPGA	
Pin No	Pin Name		Pin No.	Bank
B3	GND	GND	-	-
B4	DP9_M2C_P	HPC_DP9_M2C_P	B31	1J
B5	DP9_M2C_N	HPC_DP9_M2C_N	B30	1J
B6	GND	GND	-	-
B7	GND	GND	-	-
B8	DP8_M2C_P	HPC_DP8_M2C_P	D31	1J
B9	DP8_M2C_N	HPC_DP8_M2C_N	D30	1J
B10	GND	GND	-	-
B11	GND	GND	-	-
B12	DP7_M2C_P	HPC_DP7_M2C_P	E33	1J
B13	DP7_M2C_N	HPC_DP7_M2C_N	E32	1J
B14	GND	GND	-	-
B15	GND	GND	-	-
B16	DP6_M2C_P	HPC_DP6_M2C_P	F31	1J
B17	DP6_M2C_N	HPC_DP6_M2C_N	F30	1J
B18	GND	GND	-	-
B19	GND	GND	-	-
B20	GBTCLK1_M2C_P	HPC_GBTCLK1_M2C_P	E29	1J
B21	GBTCLK1_M2C_N	HPC_GBTCLK1_M2C_N	E28	1J
B22	GND	GND	-	-
B23	GND	GND	-	-
B24	DP9_C2M_P	HPC_DP9_C2M_P	A33	1J
B25	DP9_C2M_N	HPC_DP9_C2M_N	A32	1J
B26	GND	GND	-	-
B27	GND	GND	-	-
B28	DP8_C2M_P	HPC_DP8_C2M_P	C33	1J
B29	DP8_C2M_N	HPC_DP8_C2M_N	C32	1J
B30	GND	GND	-	-
B31	GND	GND	-	-
B32	DP7_C2M_P	HPC_DP7_C2M_P	B35	1J
B33	DP7_C2M_N	HPC_DP7_C2M_N	B34	1J
B34	GND	GND	-	-
B35	GND	GND	-	-
B36	DP6_C2M_P	HPC_DP6_C2M_P	A37	1J
B37	DP6_C2M_N	HPC_DP6_C2M_N	A36	1J
B38	GND	GND	-	-
B39	GND	GND	-	-
B40	RES0	RES0	-	-
C1	GND	GND	-	-
C2	DP0_C2M_P	HPC_DP0_C2M_P	F35	1I
C3	DP0_C2M_N	HPC_DP0_C2M_N	F34	1I
C4	GND	GND	-	-
C5	GND	GND	-	-
C6	DP0_M2C_P	HPC_DP0_M2C_P	K35	1I
C7	DP0_M2C_N	HPC_DP0_M2C_N	K34	1I
C8	GND	GND	-	-
C9	GND	GND	-	-

CN7		Signal Name	FPGA	
Pin No	Pin Name		Pin No.	Bank
C10	LA06_P	HPC_LA06_P	L14	3H
C11	LA06_N	HPC_LA06_N	L15	3H
C12	GND	GND	-	-
C13	GND	GND	-	-
C14	LA10_P	HPC_LA10_P	G14	3H
C15	LA10_N	HPC_LA10_N	H14	3H
C16	GND	GND	-	-
C17	GND	GND	-	-
C18	LA14_P	HPC_LA14_P	C14	3H
C19	LA14_N	HPC_LA14_N	D14	3H
C20	GND	GND	-	-
C21	GND	GND	-	-
C22	LA18_P_CC	HPC_LA18_P	B11	3H
C23	LA18_N_CC	HPC_LA18_N	B12	3H
C24	GND	GND	-	-
C25	GND	GND	-	-
C26	LA27_P	HPC_LA27_P	A9	3H
C27	LA27_N	HPC_LA27_N	B9	3H
C28	GND	GND	-	-
C29	GND	GND	-	-
C30	SCL	HPC_SCL	A8	3H
C31	SDA	HPC_SDA	A7	3H
C32	GND	GND	-	-
C33	GND	GND	-	-
C34	GA0	HPC_GA0	D9	3H
C35	12P0V	IN+12V	-	-
C36	GND	GND	-	-
C37	12P0V	IN+12V	-	-
C38	GND	GND	-	-
C39	3P3V	BD+3p3v	-	-
C40	GND	GND	-	-
D1	PG_C2M	Pull Up to BD+3p3v	-	-
D2	GND	GND	-	-
D3	GND	GND	-	-
D4	GBTCLK0_M2C_P	HPC_GBTCLK0_M2C_P	J29	1I
D5	GBTCLK0_M2C_N	HPC_GBTCLK0_M2C_N	J28	1I
D6	GND	GND	AR20	2A
D7	GND	GND	AR20	2A
D8	LA01_P_CC	HPC_LA01_P_CC	F13	3H
D9	LA01_N_CC	HPC_LA01_N_CC	F14	3H
D10	GND	GND	AR20	2A
D11	LA05_P	HPC_LA05_P	L12	3H
D12	LA05_N	HPC_LA05_N	L13	3H
D13	GND	GND	AR20	2A
D14	LA09_P	HPC_LA09_P	J13	3H
D15	LA09_N	HPC_LA09_N	J14	3H
D16	GND	GND	AR20	2A

CN7		Signal Name	FPGA	
Pin No	Pin Name		Pin No.	Bank
D17	LA13_P	HPC_LA13_P	F12	3H
D18	LA13_N	HPC_LA13_N	G12	3H
D19	GND	GND	AR20	2A
D20	LA17_P_CC	HPC_LA17_P	E12	3H
D21	LA17_N_CC	HPC_LA17_N	E13	3H
D22	GND	GND	AR20	2A
D23	LA23_P	HPC_LA23_P	A10	3H
D24	LA23_N	HPC_LA23_N	B10	3H
D25	GND	GND	AR20	2A
D26	LA26_P	HPC_LA26_P	D10	3H
D27	LA26_N	HPC_LA26_N	E10	3H
D28	GND	GND	AR20	2A
D29	TCK	HPC_TCK(From U26)	-	-
D30	TDI	HPC_TDI(From U26)	-	-
D31	TDO	HPC_TDO(To CN7,U28)	-	-
D32	3P3VAUX	BD+3p3v	-	-
D33	TMS	HPC_TMS(From U26)	-	-
D34	TRST_L	-	-	-
D35	GA1	HPC_GA1	C9	3H
D36	3P3V	BD+3p3v	-	-
D37	GND	GND	-	-
D38	3P3V	BD+3p3v	-	-
D39	GND	GND	-	-
D40	3P3V	BD+3p3v	-	-
E1	GND	GND	-	-
E2	HA01_P_CC	HPC_HA01_P_CC	E5	3G
E3	HA01_N_CC	HPC_HA01_N_CC	F5	3G
E4	GND	GND	-	-
E5	GND	GND	-	-
E6	HA05_P	HPC_HA05_P	M12	3G
E7	HA05_N	HPC_HA05_N	N13	3G
E8	GND	GND	-	-
E9	HA09_P	HPC_HA09_P	M10	3G
E10	HA09_N	HPC_HA09_N	N11	3G
E11	GND	GND	-	-
E12	HA13_P	HPC_HA13_P	K10	3G
E13	HA13_N	HPC_HA13_N	L10	3G
E14	GND	GND	-	-
E15	HA16_P	HPC_HA16_P	F9	3G
E16	HA16_N	HPC_HA16_N	G9	3G
E17	GND	GND	-	-
E18	HA20_P	HPC_HA20_P	J8	3G
E19	HA20_N	HPC_HA20_N	K8	3G
E20	GND	GND	-	-
E21	HB03_P	HPC_HB03_P	C8	3G
E22	HB03_N	HPC_HB03_N	D8	3G
E23	GND	GND	-	-

CN7		Signal Name	FPGA	
Pin No	Pin Name		Pin No.	Bank
E24	HB05_P	HPC_HB05_P	B7	3G
E25	HB05_N	HPC_HB05_N	C7	3G
E26	GND	GND	-	-
E27	HB09_P	HPC_HB09_P	B6	3G
E28	HB09_N	HPC_HB09_N	C6	3G
E29	GND	GND	-	-
E30	HB13_P	HPC_HB13_P	G5	3G
E31	HB13_N	HPC_HB13_N	G6	3G
E32	GND	GND	-	-
E33	HB19_P	HPC_HB19_P	C3	3G
E34	HB19_N	HPC_HB19_N	C4	3G
E35	GND	GND	-	-
E36	HB21_P	HPC_HB21_P	H6	3G
E37	HB21_N	HPC_HB21_N	J6	3G
E38	GND	GND	-	-
E39	VADJ	FP+1p8v-2	-	-
E40	GND	GND	-	-
F1	PG M2C	Pull Up to BD+3p3v	-	-
F2	GND	GND	-	-
F3	GND	GND	-	-
F4	HA00_P_CC	HPC_HA00_P_CC	H8	3G
F5	HA00_N_CC	HPC_HA00_N_CC	H9	3G
F6	GND	GND	-	-
F7	HA04_P	HPC_HA04_P	M11	3G
F8	HA04_N	HPC_HA04_N	N12	3G
F9	GND	GND	-	-
F10	HA08_P	HPC_HA08_P	J11	3G
F11	HA08_N	HPC_HA08_N	K11	3G
F12	GND	GND	-	-
F13	HA12_P	HPC_HA12_P	J9	3G
F14	HA12_N	HPC_HA12_N	J10	3G
F15	GND	GND	-	-
F16	HA15_P	HPC_HA15_P	E8	3G
F17	HA15_N	HPC_HA15_N	F8	3G
F18	GND	GND	-	-
F19	HA19_P	HPC_HA19_P	G7	3G
F20	HA19_N	HPC_HA19_N	H7	3G
F21	GND	GND	-	-
F22	HB02_P	HPC_HB02_P	E7	3G
F23	HB02_N	HPC_HB02_N	F7	3G
F24	GND	GND	-	-
F25	HB04_P	HPC_HB04_P	D4	3G
F26	HB04_N	HPC_HB04_N	D5	3G
F27	GND	GND	-	-
F28	HB08_P	HPC_HB08_P	D6	3G
F29	HB08_N	HPC_HB08_N	E6	3G
F30	GND	GND	-	-

CN7		Signal Name	FPGA	
Pin No	Pin Name		Pin No.	Bank
F31	HB12_P	HPC_HB12_P	A4	3G
F32	HB12_N	HPC_HB12_N	B4	3G
F33	GND	GND	-	-
F34	HB16_P	HPC_HB16_P	C2	3G
F35	HB16_N	HPC_HB16_N	D3	3G
F36	GND	GND	-	-
F37	HB20_P	HPC_HB20_P	A5	3G
F38	HB20_N	HPC_HB20_N	B5	3G
F39	GND	GND	-	-
F40	VADJ	FP+1p8v-2	-	-
G1	GND	GND	-	-
G2	CLK1_M2C_P	HPC_CLK1_M2C_P	K18	2L
G3	CLK1_M2C_N	HPC_CLK1_M2C_N	L19	2L
G4	GND	GND	-	-
G5	GND	GND	-	-
G6	LA00_P_CC	HPC_LA00_P_CC	C11	3H
G7	LA00_N_CC	HPC_LA00_N_CC	C12	3H
G8	GND	GND	-	-
G9	LA03_P	HPC_LA03_P	K22	2L
G10	LA03_N	HPC_LA03_N	L22	2L
G11	GND	GND	-	-
G12	LA08_P	HPC_LA08_P	H23	2L
G13	LA08_N	HPC_LA08_N	J23	2L
G14	GND	GND	-	-
G15	LA12_P	HPC_LA12_P	G20	2L
G16	LA12_N	HPC_LA12_N	G21	2L
G17	GND	GND	-	-
G18	LA16_P	HPC_LA16_P	E21	2L
G19	LA16_N	HPC_LA16_N	E22	2L
G20	GND	GND	-	-
G21	LA20_P	HPC_LA20_P	D21	2L
G22	LA20_N	HPC_LA20_N	D20	2L
G23	GND	GND	-	-
G24	LA22_P	HPC_LA22_P	F18	2L
G25	LA22_N	HPC_LA22_N	G17	2L
G26	GND	GND	-	-
G27	LA25_P	HPC_LA25_P	J21	2L
G28	LA25_N	HPC_LA25_N	J20	2L
G29	GND	GND	-	-
G30	LA29_P	HPC_LA29_P	H18	2L
G31	LA29_N	HPC_LA29_N	H19	2L
G32	GND	GND	-	-
G33	LA31_P	HPC_LA31_P	M22	2L
G34	LA31_N	HPC_LA31_N	M21	2L
G35	GND	GND	-	-
G36	LA33_P	HPC_LA33_P	N23	2L
G37	LA33_N	HPC_LA33_N	N22	2L

CN7		Signal Name	FPGA	
Pin No	Pin Name		Pin No.	Bank
G38	GND	GND	-	-
G39	VADJ	FP+1p8v-2	-	-
G40	GND	GND	-	-
H1	VREF_A_M2C	-	-	-
H2	PRSNT_M2C_L	HPC_PRSNT_M2C_L(To U27)	-	-
H3	GND	GND	-	-
H4	CLK0_M2C_P	HPC_CLK0_M2C_P	F22	2L
H5	CLK0_M2C_N	HPC_CLK0_M2C_N	G22	2L
H6	GND	GND	-	-
H7	LA02_P	HPC_LA02_P	K23	2L
H8	LA02_N	HPC_LA02_N	L23	2L
H9	GND	GND	-	-
H10	LA04_P	HPC_LA04_P	K21	2L
H11	LA04_N	HPC_LA04_N	K20	2L
H12	GND	GND	-	-
H13	LA07_P	HPC_LA07_P	H22	2L
H14	LA07_N	HPC_LA07_N	H21	2L
H15	GND	GND	-	-
H16	LA11_P	HPC_LA11_P	E20	2L
H17	LA11_N	HPC_LA11_N	F20	2L
H18	GND	GND	-	-
H19	LA15_P	HPC_LA15_P	F19	2L
H20	LA15_N	HPC_LA15_N	G19	2L
H21	GND	GND	-	-
H22	LA19_P	HPC_LA19_P	C19	2L
H23	LA19_N	HPC_LA19_N	D19	2L
H24	GND	GND	-	-
H25	LA21_P	HPC_LA21_P	C17	2L
H26	LA21_N	HPC_LA21_N	C18	2L
H27	GND	GND	-	-
H28	LA24_P	HPC_LA24_P	E17	2L
H29	LA24_N	HPC_LA24_N	F17	2L
H30	GND	GND	-	-
H31	LA28_P	HPC_LA28_P	J18	2L
H32	LA28_N	HPC_LA28_N	J19	2L
H33	GND	GND	-	-
H34	LA30_P	HPC_LA30_P	L20	2L
H35	LA30_N	HPC_LA30_N	M20	2L
H36	GND	GND	-	-
H37	LA32_P	HPC_LA32_P	N20	2L
H38	LA32_N	HPC_LA32_N	P20	2L
H39	GND	GND	-	-
H40	VADJ	FP+1p8v-2	-	-
J1	GND	GND	-	-
J2	CLK3_M2C_P	HPC_CLK3_M2C_P	F25	2K
J3	CLK3_M2C_N	HPC_CLK3_M2C_N	G24	2K
J4	GND	GND	-	-

CN7		Signal Name	FPGA	
Pin No	Pin Name		Pin No.	Bank
J5	GND	GND	-	-
J6	HA03_P	HPC_HA03_P	N25	2K
J7	HA03_N	HPC_HA03_N	P25	2K
J8	GND	GND	-	-
J9	HA07_P	HPC_HA07_P	K26	2K
J10	HA07_N	HPC_HA07_N	L26	2K
J11	GND	GND	-	-
J12	HA11_P	HPC_HA11_P	E26	2K
J13	HA11_N	HPC_HA11_N	F26	2K
J14	GND	GND	-	-
J15	HA14_P	HPC_HA14_P	B26	2K
J16	HA14_N	HPC_HA14_N	C26	2K
J17	GND	GND	-	-
J18	HA18_P	HPC_HA18_P	A26	2K
J19	HA18_N	HPC_HA18_N	A25	2K
J20	GND	GND	-	-
J21	HA22_P	HPC_HA22_P	A24	2K
J22	HA22_N	HPC_HA22_N	A23	2K
J23	GND	GND	-	-
J24	HB01_P	HPC_HB01_P	A22	2K
J25	HB01_N	HPC_HB01_N	B21	2K
J26	GND	GND	-	-
J27	HB07_P	HPC_HB07_P	C22	2K
J28	HB07_N	HPC_HB07_N	C21	2K
J29	GND	GND	-	-
J30	HB11_P	HPC_HB11_P	B20	2K
J31	HB11_N	HPC_HB11_N	B19	2K
J32	GND	GND	-	-
J33	HB15_P	HPC_HB15_P	J26	2K
J34	HB15_N	HPC_HB15_N	J25	2K
J35	GND	GND	-	-
J36	HB18_P	HPC_HB18_P	K25	2K
J37	HB18_N	HPC_HB18_N	L24	2K
J38	GND	GND	-	-
J39	VIO_B_M2C	-	-	-
J40	GND	GND	-	-
K1	VREF_B_M2C	-	-	-
K2	GND	GND	-	-
K3	GND	GND	-	-
K4	CLK2_M2C_P	HPC_CLK2_M2C_P	C24	2K
K5	CLK2_M2C_N	HPC_CLK2_M2C_N	D24	2K
K6	GND	GND	-	-
K7	HA02_P	HPC_HA02_P	M24	2K
K8	HA02_N	HPC_HA02_N	N24	2K
K9	GND	GND	-	-
K10	HA06_P	HPC_HA06_P	F24	2K
K11	HA06_N	HPC_HA06_N	F23	2K

CN7		Signal Name	FPGA	
Pin No	Pin Name		Pin No.	Bank
K12	GND	GND	-	-
K13	HA10_P	HPC_HA10_P	D25	2K
K14	HA10_N	HPC_HA10_N	E25	2K
K15	GND	GND	-	-
K16	HA17_P_CC	HPC_HA17_P_CC	B22	2K
K17	HA17_N_CC	HPC_HA17_N_CC	C23	2K
K18	GND	GND	-	-
K19	HA21_P	HPC_HA21_P	C25	2K
K20	HA21_N	HPC_HA21_N	B24	2K
K21	GND	GND	-	-
K22	HA23_P	HPC_HA23_P	D23	2K
K23	HA23_N	HPC_HA23_N	E23	2K
K24	GND	GND	-	-
K25	HB00_P_CC	HPC_HB00_P_CC	G26	2K
K26	HB00_N_CC	HPC_HB00_N_CC	G25	2K
K27	GND	GND	-	-
K28	HB06_P_CC	HPC_HB06_P	A20	2K
K29	HB06_N_CC	HPC_HB06_N	A19	2K
K30	GND	GND	-	-
K31	HB10_P	HPC_HB10_P	A17	2K
K32	HB10_N	HPC_HB10_N	A18	2K
K33	GND	GND	-	-
K34	HB14_P	HPC_HB14_P	H24	2K
K35	HB14_N	HPC_HB14_N	J24	2K
K36	GND	GND	-	-
K37	HB17_P_CC	HPC_HB17_P	L25	2K
K38	HB17_N_CC	HPC_HB17_N	M25	2K
K39	GND	GND	-	-
K40	VIO_B_M2C	-	-	-

7.2.5.3. FMC Connector (LPC) Pin Assignment Table

The following table shows the pin assignments for the FPGA and CN9.

Table 7.2.5-3 FPGA-FMC Connector (CN9) Pin Assignment

CN9		Signal Name	FPGA	
Pin No	Pin Name		Pin No.	Bank
A1	GND	-	-	-
A2	DP1_M2C_P	-	-	-
A3	DP1_M2C_N	-	-	-
A4	GND	-	-	-
A5	GND	-	-	-
A6	DP2_M2C_P	-	-	-
A7	DP2_M2C_N	-	-	-
A8	GND	-	-	-
A9	GND	-	-	-
A10	DP3_M2C_P	-	-	-
A11	DP3_M2C_N	-	-	-
A12	GND	-	-	-
A13	GND	-	-	-
A14	DP4_M2C_P	-	-	-
A15	DP4_M2C_N	-	-	-
A16	GND	-	-	-
A17	GND	-	-	-
A18	DP5_M2C_P	-	-	-
A19	DP5_M2C_N	-	-	-
A20	GND	-	-	-
A21	GND	-	-	-
A22	DP1_C2M_P	-	-	-
A23	DP1_C2M_N	-	-	-
A24	GND	-	-	-
A25	GND	-	-	-
A26	DP2_C2M_P	-	-	-
A27	DP2_C2M_N	-	-	-
A28	GND	-	-	-
A29	GND	-	-	-
A30	DP3_C2M_P	-	-	-
A31	DP3_C2M_N	-	-	-
A32	GND	-	-	-
A33	GND	-	-	-
A34	DP4_C2M_P	-	-	-
A35	DP4_C2M_N	-	-	-
A36	GND	-	-	-
A37	GND	-	-	-
A38	DP5_C2M_P	-	-	-
A39	DP5_C2M_N	-	-	-
A40	GND	-	-	-
B1	RES1	-	-	-

CN9		Signal Name	FPGA	
Pin No	Pin Name		Pin No.	Bank
B2	GND	-	-	-
B3	GND	-	-	-
B4	DP9_M2C_P	-	-	-
B5	DP9_M2C_N	-	-	-
B6	GND	-	-	-
B7	GND	-	-	-
B8	DP8_M2C_P	-	-	-
B9	DP8_M2C_N	-	-	-
B10	GND	-	-	-
B11	GND	-	-	-
B12	DP7_M2C_P	-	-	-
B13	DP7_M2C_N	-	-	-
B14	GND	-	-	-
B15	GND	-	-	-
B16	DP6_M2C_P	-	-	-
B17	DP6_M2C_N	-	-	-
B18	GND	-	-	-
B19	GND	-	-	-
B20	GBTCLK1_M2C_P	-	-	-
B21	GBTCLK1_M2C_N	-	-	-
B22	GND	-	-	-
B23	GND	-	-	-
B24	DP9_C2M_P	-	-	-
B25	DP9_C2M_N	-	-	-
B26	GND	-	-	-
B27	GND	-	-	-
B28	DP8_C2M_P	-	-	-
B29	DP8_C2M_N	-	-	-
B30	GND	-	-	-
B31	GND	-	-	-
B32	DP7_C2M_P	-	-	-
B33	DP7_C2M_N	-	-	-
B34	GND	-	-	-
B35	GND	-	-	-
B36	DP6_C2M_P	-	-	-
B37	DP6_C2M_N	-	-	-
B38	GND	-	-	-
B39	GND	-	-	-
B40	RES0	-	-	-
C1	GND	GND	-	-
C2	DP0_C2M_P	LPC_DP0_C2M_P	AL37	1E
C3	DP0_C2M_N	LPC_DP0_C2M_N	AL36	1E
C4	GND	GND	-	-
C5	GND	GND	-	-
C6	DP0_M2C_P	LPC_DP0_M2C_P	AH35	1E
C7	DP0_M2C_N	LPC_DP0_M2C_N	AH34	1E
C8	GND	GND	-	-

CN9		Signal Name	FPGA	
Pin No	Pin Name		Pin No.	Bank
C9	GND	GND	-	-
C10	LA06_P	LPC_LA06_P	AR8	3A
C11	LA06_N	LPC_LA06_N	AP8	3A
C12	GND	GND	-	-
C13	GND	GND	-	-
C14	LA10_P	LPC_LA10_P	AV7	3A
C15	LA10_N	LPC_LA10_N	AU7	3A
C16	GND	GND	-	-
C17	GND	GND	-	-
C18	LA14_P	LPC_LA14_P	AV9	3A
C19	LA14_N	LPC_LA14_N	AU9	3A
C20	GND	GND	-	-
C21	GND	GND	-	-
C22	LA18_P_CC	LPC_LA18_P_CC	AR10	3A
C23	LA18_N_CC	LPC_LA18_N_CC	AP10	3A
C24	GND	GND	-	-
C25	GND	GND	-	-
C26	LA27_P	LPC_LA27_P	AT9	3A
C27	LA27_N	LPC_LA27_N	AT10	3A
C28	GND	GND	-	-
C29	GND	GND	-	-
C30	SCL	LPC_SCL	AJ14	3A
C31	SDA	LPC_SDA	AH14	3A
C32	GND	GND	-	-
C33	GND	GND	-	-
C34	GA0	LPC_GA0	AF15	3A
C35	12P0V	IN+12V	-	-
C36	GND	GND	-	-
C37	12P0V	IN+12V	-	-
C38	GND	GND	-	-
C39	3P3V	BD+3P3V	-	-
C40	GND	GND	-	-
D1	PG_C2M	Pull Up to BD+3p3	-	-
D2	GND	GND	-	-
D3	GND	GND	-	-
D4	GBTCLK0_M2C_P	LPC_GBTCLK0_M2C_P	AG29	1E
D5	GBTCLK0_M2C_N	LPC_GBTCLK0_M2C_N	AG28	1E
D6	GND	GND	-	-
D7	GND	GND	-	-
D8	LA01_P_CC	LPC_LA01_P_CC	AR11	3A
D9	LA01_N_CC	LPC_LA01_N_CC	AP11	3A
D10	GND	GND	-	-
D11	LA05_P	LPC_LA05_P	AT7	3A
D12	LA05_N	LPC_LA05_N	AT8	3A
D13	GND	GND	-	-
D14	LA09_P	LPC_LA09_P	AU1	3B
D15	LA09_N	LPC_LA09_N	AU2	3B

CN9		Signal Name	FPGA	
Pin No	Pin Name		Pin No.	Bank
D16	GND	GND	-	-
D17	LA13_P	LPC_LA13_P	AW8	3A
D18	LA13_N	LPC_LA13_N	AV8	3A
D19	GND	GND	-	-
D20	LA17_P_CC	LPC_LA17_P_CC	AM12	3A
D21	LA17_N_CC	LPC_LA17_N_CC	AL12	3A
D22	GND	GND	-	-
D23	LA23_P	LPC_LA23_P	AW9	3A
D24	LA23_N	LPC_LA23_N	AW10	3A
D25	GND	GND	-	-
D26	LA26_P	LPC_LA26_P	AU10	3A
D27	LA26_N	LPC_LA26_N	AU11	3A
D28	GND	GND	-	-
D29	TCK	LPC_TCK(From U26)	-	-
D30	TDI	LPC_TDI(From U27,U28,CN7)	-	-
D31	TDO	LPC_TDO(To CN8)	-	-
D32	3P3VAUX	BD+3P3V	-	-
D33	TMS	LPC_TMS(From U26)	-	-
D34	TRST_L	-	-	-
D35	GA1	LPC_GA1	AG15	3A
D36	3P3V	BD+3P3V	-	-
D37	GND	GND	-	-
D38	3P3V	BD+3P3V	-	-
D39	GND	GND	-	-
D40	3P3V	BD+3P3V	-	-
E1	GND	-	-	-
E2	HA01_P_CC	-	-	-
E3	HA01_N_CC	-	-	-
E4	GND	-	-	-
E5	GND	-	-	-
E6	HA05_P	-	-	-
E7	HA05_N	-	-	-
E8	GND	-	-	-
E9	HA09_P	-	-	-
E10	HA09_N	-	-	-
E11	GND	-	-	-
E12	HA13_P	-	-	-
E13	HA13_N	-	-	-
E14	GND	-	-	-
E15	HA16_P	-	-	-
E16	HA16_N	-	-	-
E17	GND	-	-	-
E18	HA20_P	-	-	-
E19	HA20_N	-	-	-
E20	GND	-	-	-
E21	HB03_P	-	-	-
E22	HB03_N	-	-	-

CN9		Signal Name	FPGA	
Pin No	Pin Name		Pin No.	Bank
E23	GND	-	-	-
E24	HB05_P	-	-	-
E25	HB05_N	-	-	-
E26	GND	-	-	-
E27	HB09_P	-	-	-
E28	HB09_N	-	-	-
E29	GND	-	-	-
E30	HB13_P	-	-	-
E31	HB13_N	-	-	-
E32	GND	-	-	-
E33	HB19_P	-	-	-
E34	HB19_N	-	-	-
E35	GND	-	-	-
E36	HB21_P	-	-	-
E37	HB21_N	-	-	-
E38	GND	-	-	-
E39	VADJ	-	-	-
E40	GND	-	-	-
F1	PG M2C	-	-	-
F2	GND	-	-	-
F3	GND	-	-	-
F4	HA00_P_CC	-	-	-
F5	HA00_N_CC	-	-	-
F6	GND	-	-	-
F7	HA04_P	-	-	-
F8	HA04_N	-	-	-
F9	GND	-	-	-
F10	HA08_P	-	-	-
F11	HA08_N	-	-	-
F12	GND	-	-	-
F13	HA12_P	-	-	-
F14	HA12_N	-	-	-
F15	GND	-	-	-
F16	HA15_P	-	-	-
F17	HA15_N	-	-	-
F18	GND	-	-	-
F19	HA19_P	-	-	-
F20	HA19_N	-	-	-
F21	GND	-	-	-
F22	HB02_P	-	-	-
F23	HB02_N	-	-	-
F24	GND	-	-	-
F25	HB04_P	-	-	-
F26	HB04_N	-	-	-
F27	GND	-	-	-
F28	HB08_P	-	-	-
F29	HB08_N	-	-	-

CN9		Signal Name	FPGA	
Pin No	Pin Name		Pin No.	Bank
F30	GND	-	-	-
F31	HB12_P	-	-	-
F32	HB12_N	-	-	-
F33	GND	-	-	-
F34	HB16_P	-	-	-
F35	HB16_N	-	-	-
F36	GND	-	-	-
F37	HB20_P	-	-	-
F38	HB20_N	-	-	-
F39	GND	-	-	-
F40	VADJ	-	-	-
G1	GND	GND	-	-
G2	CLK1_M2C_P	LPC_CLK1_M2C_P	AL9	3B
G3	CLK1_M2C_N	LPC_CLK1_M2C_N	AK10	3B
G4	GND	GND	-	-
G5	GND	GND	-	-
G6	LA00_P_CC	LPC_LA00_P_CC	AM10	3A
G7	LA00_N_CC	LPC_LA00_N_CC	AL10	3A
G8	GND	GND	-	-
G9	LA03_P	LPC_LA03_P	AN6	3B
G10	LA03_N	LPC_LA03_N	AM6	3B
G11	GND	GND	-	-
G12	LA08_P	LPC_LA08_P	AR5	3B
G13	LA08_N	LPC_LA08_N	AP6	3B
G14	GND	GND	-	-
G15	LA12_P	LPC_LA12_P	AT2	3B
G16	LA12_N	LPC_LA12_N	AT3	3B
G17	GND	GND	-	-
G18	LA16_P	LPC_LA16_P	AP4	3B
G19	LA16_N	LPC_LA16_N	AP5	3B
G20	GND	GND	-	-
G21	LA20_P	LPC_LA20_P	AU5	3B
G22	LA20_N	LPC_LA20_N	AU6	3B
G23	GND	GND	-	-
G24	LA22_P	LPC_LA22_P	AR6	3B
G25	LA22_N	LPC_LA22_N	AR7	3B
G26	GND	GND	-	-
G27	LA25_P	LPC_LA25_P	AL8	3B
G28	LA25_N	LPC_LA25_N	AK8	3B
G29	GND	GND	-	-
G30	LA29_P	LPC_LA29_P	AN8	3B
G31	LA29_N	LPC_LA29_N	AM9	3B
G32	GND	GND	-	-
G33	LA31_P	LPC_LA31_P	AJ10	3B
G34	LA31_N	LPC_LA31_N	AJ11	3B
G35	GND	GND	-	-
G36	LA33_P	LPC_LA33_P	AH11	3B

CN9		Signal Name	FPGA	
Pin No	Pin Name		Pin No.	Bank
G37	LA33_N	LPC_LA33_N	AG11	3B
G38	GND	GND	-	-
G39	VADJ	FP+1P8V-3	-	-
G40	GND	GND	-	-
H1	VREF_A_M2C	-	-	-
H2	PRSNT_M2C_L	LPC_PRSNT_M2C_L(To U27)	-	-
H3	GND	GND	-	-
H4	CLK0_M2C_P	LPC_CLK0_M2C_P	AN4	3B
H5	CLK0_M2C_N	LPC_CLK0_M2C_N	AM5	3B
H6	GND	GND	-	-
H7	LA02_P	LPC_LA02_P	AL7	3B
H8	LA02_N	LPC_LA02_N	AK7	3B
H9	GND	GND	-	-
H10	LA04_P	LPC_LA04_P	AR3	3B
H11	LA04_N	LPC_LA04_N	AP3	3B
H12	GND	GND	-	-
H13	LA07_P	LPC_LA07_P	AV4	3B
H14	LA07_N	LPC_LA07_N	AU4	3B
H15	GND	GND	-	-
H16	LA11_P	LPC_LA11_P	AT4	3B
H17	LA11_N	LPC_LA11_N	AT5	3B
H18	GND	GND	-	-
H19	LA15_P	LPC_LA15_P	AW4	3B
H20	LA15_N	LPC_LA15_N	AW5	3B
H21	GND	GND	-	-
H22	LA19_P	LPC_LA19_P	AW6	3B
H23	LA19_N	LPC_LA19_N	AV6	3B
H24	GND	GND	-	-
H25	LA21_P	LPC_LA21_P	AN7	3B
H26	LA21_N	LPC_LA21_N	AM7	3B
H27	GND	GND	-	-
H28	LA24_P	LPC_LA24_P	AJ8	3B
H29	LA24_N	LPC_LA24_N	AH8	3B
H30	GND	GND	-	-
H31	LA28_P	LPC_LA28_P	AJ9	3B
H32	LA28_N	LPC_LA28_N	AH9	3B
H33	GND	GND	-	-
H34	LA30_P	LPC_LA30_P	AG9	3B
H35	LA30_N	LPC_LA30_N	AG10	3B
H36	GND	GND	-	-
H37	LA32_P	LPC_LA32_P	AG12	3B
H38	LA32_N	LPC_LA32_N	AF12	3B
H39	GND	GND	-	-
H40	VADJ	FP+1P8V-3	-	-
J1	GND	-	-	-
J2	CLK3_M2C_P	-	-	-
J3	CLK3_M2C_N	-	-	-

CN9		Signal Name	FPGA	
Pin No	Pin Name		Pin No.	Bank
J4	GND	-	-	-
J5	GND	-	-	-
J6	HA03_P	-	-	-
J7	HA03_N	-	-	-
J8	GND	-	-	-
J9	HA07_P	-	-	-
J10	HA07_N	-	-	-
J11	GND	-	-	-
J12	HA11_P	-	-	-
J13	HA11_N	-	-	-
J14	GND	-	-	-
J15	HA14_P	-	-	-
J16	HA14_N	-	-	-
J17	GND	-	-	-
J18	HA18_P	-	-	-
J19	HA18_N	-	-	-
J20	GND	-	-	-
J21	HA22_P	-	-	-
J22	HA22_N	-	-	-
J23	GND	-	-	-
J24	HB01_P	-	-	-
J25	HB01_N	-	-	-
J26	GND	-	-	-
J27	HB07_P	-	-	-
J28	HB07_N	-	-	-
J29	GND	-	-	-
J30	HB11_P	-	-	-
J31	HB11_N	-	-	-
J32	GND	-	-	-
J33	HB15_P	-	-	-
J34	HB15_N	-	-	-
J35	GND	-	-	-
J36	HB18_P	-	-	-
J37	HB18_N	-	-	-
J38	GND	-	-	-
J39	VIO_B_M2C	-	-	-
J40	GND	-	-	-
K1	VREF_B_M2C	-	-	-
K2	GND	-	-	-
K3	GND	-	-	-
K4	CLK2_M2C_P	-	-	-
K5	CLK2_M2C_N	-	-	-
K6	GND	-	-	-
K7	HA02_P	-	-	-
K8	HA02_N	-	-	-
K9	GND	-	-	-
K10	HA06_P	-	-	-

CN9		Signal Name	FPGA	
Pin No	Pin Name		Pin No.	Bank
K11	HA06_N	-	-	-
K12	GND	-	-	-
K13	HA10_P	-	-	-
K14	HA10_N	-	-	-
K15	GND	-	-	-
K16	HA17_P_CC	-	-	-
K17	HA17_N_CC	-	-	-
K18	GND	-	-	-
K19	HA21_P	-	-	-
K20	HA21_N	-	-	-
K21	GND	-	-	-
K22	HA23_P	-	-	-
K23	HA23_N	-	-	-
K24	GND	-	-	-
K25	HB00_P_CC	-	-	-
K26	HB00_N_CC	-	-	-
K27	GND	-	-	-
K28	HB06_P_CC	-	-	-
K29	HB06_N_CC	-	-	-
K30	GND	-	-	-
K31	HB10_P	-	-	-
K32	HB10_N	-	-	-
K33	GND	-	-	-
K34	HB14_P	-	-	-
K35	HB14_N	-	-	-
K36	GND	-	-	-
K37	HB17_P_CC	-	-	-
K38	HB17_N_CC	-	-	-
K39	GND	-	-	-
K40	VIO_B_M2C	-	-	-

7.2.6.PCI Express

The FPGA and COMe module are connected to the PCI Express (PCIe).
The FPGA supports Gen2 x4 lanes, but the speed and bandwidth that can be supported are limited by the specifications of the COMe module being used.

A block diagram of the area around the FPGA and PCIe is shown below.

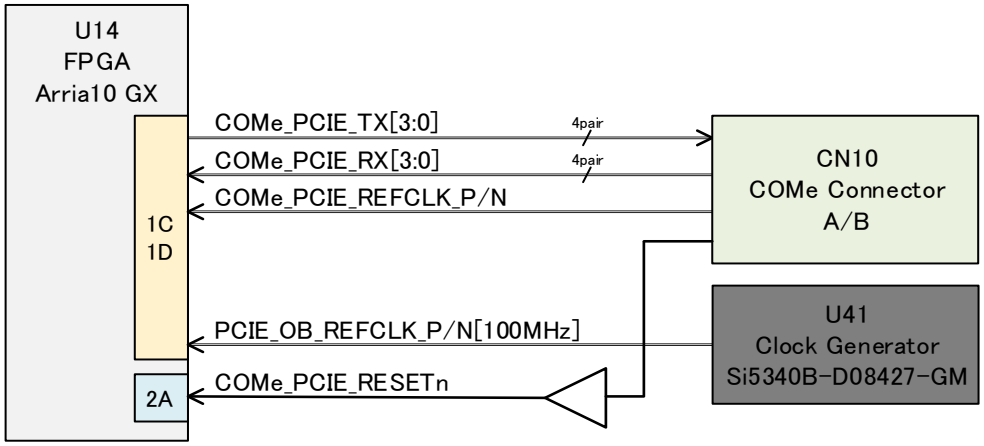

Figure 7.2.6-1 FPGA-PCIe Output Area Block Diagram

7.2.6.1. FPGA-COMe (PCIe) Pin Assignment Table

The following table shows the pin assignments for the FPGA and COMe connectors (PCIe wiring).

Table 7.2.6-1 FPGA-COMe (PCIe) Pin Assignment

CN10		Signal Name	FPGA	
Pin No.	Pin Name		Pin No	Bank
A68	PCIE_TX0+	COMe_PCIE_TX0_P	AN33	1C
A69	PCIE_TX0-	COMe_PCIE_TX0_N	AN32	1C
A64	PCIE_TX1+	COMe_PCIE_TX1_P	AM31	1C
A65	PCIE_TX1-	COMe_PCIE_TX1_N	AM30	1C
A61	PCIE_TX2+	COMe_PCIE_TX2_P	AM35	1D
A62	PCIE_TX2-	COMe_PCIE_TX2_N	AM34	1D
A58	PCIE_TX3+	COMe_PCIE_TX3_P	AL33	1D
A59	PCIE_TX3-	COMe_PCIE_TX3_N	AL32	1D
B68	PCIE_RX0+	COMe_PCIE_RX0_P	AU37	1C
B69	PCIE_RX0-	COMe_PCIE_RX0_N	AU36	1C
B64	PCIE_RX1+	COMe_PCIE_RX1_P	AT35	1C
B65	PCIE_RX1-	COMe_PCIE_RX1_N	AT34	1C
B61	PCIE_RX2+	COMe_PCIE_RX2_P	AT39	1D
B62	PCIE_RX2-	COMe_PCIE_RX2_N	AT38	1D
B58	PCIE_RX3+	COMe_PCIE_RX3_P	AR37	1D
B59	PCIE_RX3-	COMe_PCIE_RX3_N	AR36	1D
A88	PCIE_CLK_REF+	COMe_PCIE_REFCLK_P	AR29	1C
A89	PCIE_CLK_REF-	COMe_PCIE_REFCLK_N	AR28	1C
B50	CB_RESET#	COMe_PCIE_RESETn	W16	2A

7.2.7.USB UART

The board is equipped with an FT230XS (U38) manufactured by FTDI as a USB UART IC for communicating between the FPGA and PC. The PC is connected via a USB Type-B connector (CN16).
U38 and FPGA are connected by UART.

A block diagram of the area around the FPGA and USB UART is shown below.

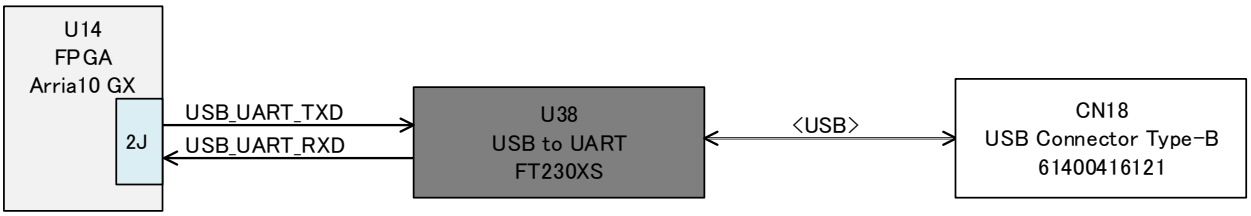

Figure 7.2.7-1 FPGA-USB UART Area Block Diagram

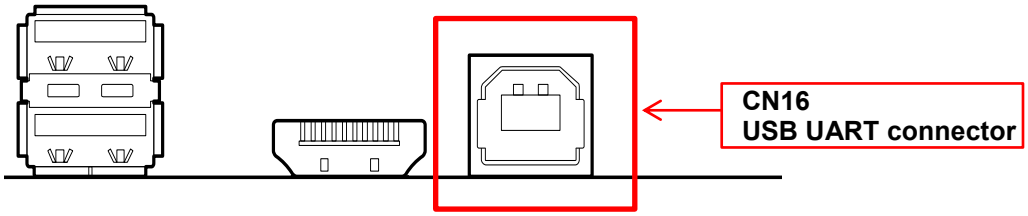

Figure 7.2.7-2 CN16

7.2.7.1. FPGA-USB UART IC Pin Assignment Table

The following table shows the pin assignments between the FPGA and USB UART IC (U38).

Table 7.2.7-1 FPGA-USB UART IC Pin Assignment

U38		Signal Name	FPGA	
Pin No	Pin Name		Pin Name	Bank
1	TXD	USB_UART_TXD	AU28	2J
4	RXD	USB_UART_RXD	AU27	2J

7.2.8.FPGA User I/F

The board is equipped with the following I/F as the user I/F for the FPGA.

- LED
  Equipped with 4 red and 4 green LED indicators
  (Lit by H output from FPGA)

- DIP switch
  Equipped with 1 8-bit DIP switch for DIP switch input
  (L is input to FPGA for each bit set to ON side)

- Push switch
  Equipped with 4 push switches for push switch input
  (L is input to FPGA when each switch is pushed)

A block diagram of the area around the FPGA and debug I/F is shown below.

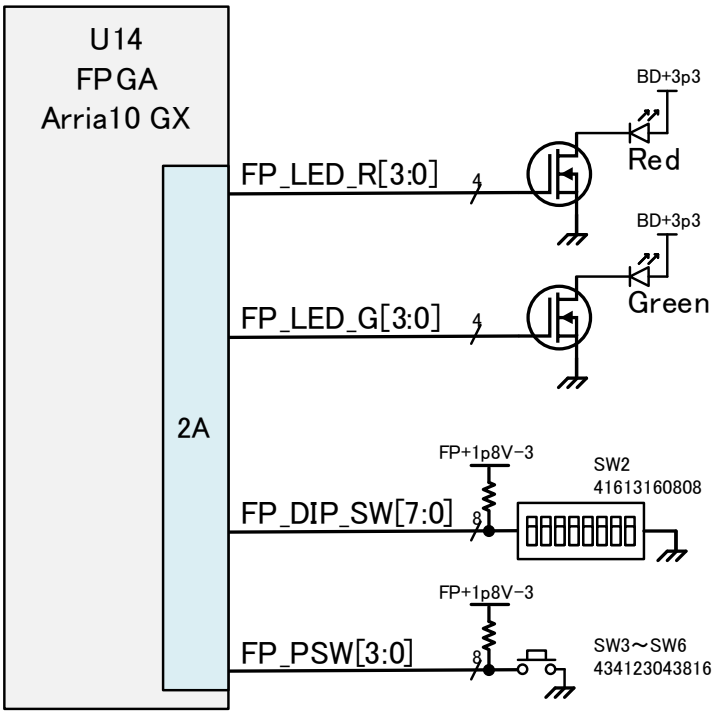

Figure 7.2.8-1 FPGA User I/F

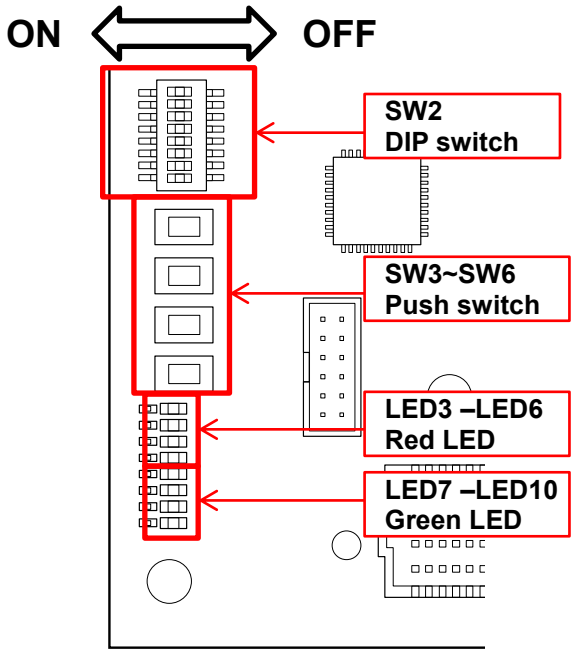

Figure 7.2.8-2 FPGA User I/F

7.2.8.1. FPGA-User I/F Pin Assignment Table

The following table shows the pin assignments between the FPGA and the user I/F.

Table 7.2.8-1 FPGA-User I/F Pin Assignment

User I/F	Reference	Signal Name	FPGA	
			Pin No	Bank
Red LED	LED3	FP_LED_R0	AU17	2A
	LED4	FP_LED_R1	AU20	2A
	LED5	FP_LED_R2	AT20	2A
	LED6	FP_LED_R3	AU19	2A
Green LED	LED7	FP_LED_G0	AR16	2A
	LED8	FP_LED_G1	AP16	2A
	LED9	FP_LED_G2	AN16	2A
	LED10	FP_LED_G3	AM16	2A
DIP switch	SW2(1pin)	FP_DIP_SW0	AM19	2A
	SW2(2pin)	FP_DIP_SW1	AM20	2A
	SW2(3pin)	FP_DIP_SW2	AN17	2A
	SW2(4pin)	FP_DIP_SW3	AM17	2A
	SW2(5pin)	FP_DIP_SW4	AL18	2A
	SW2(6pin)	FP_DIP_SW5	AL19	2A
	SW2(7pin)	FP_DIP_SW6	AJ19	2A
	SW2(8pin)	FP_DIP_SW7	AH19	2A
Push switch	SW3	FP_PSW0	AV17	2A
	SW4	FP_PSW1	AW18	2A
	SW5	FP_PSW2	AV22	2A
	SW6	FP_PSW3	AW21	2A

7.2.9.Power Connector for Fan on FPGA

The heat sink, which is provided with the product, has a cooling fan. Connect the power cable of the cooling fan to CN23 on the board.
The power connector for the fan is supplied with +12 V.

Warning	When you turn on power to the board, it will heat up, which is a characteristic of FPGA devices. This causes damage to the device, so install the heat sink and fan to cool the FPGA before you use the board.

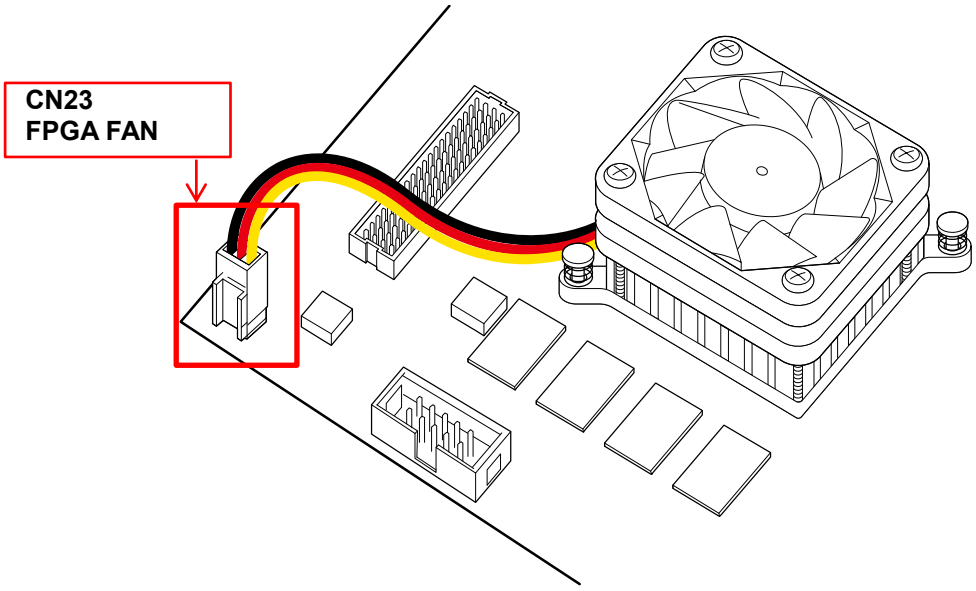

Figure 7.2.9 Installation of Heat Sink and Fan for FPGA

7.3. COM Express Type-6 Connector

The board is equipped with connectors (COMe connectors: CN10 and CN11) to which COM Express (COMe) Type-6 modules can be mounted. COM Express basic types and compact types can be mounted.
The following shows the COM Express functions that can be evaluated with this board.

- Gigabit Ethernet
- HDMI image output
- USB3.0
- SATA
- CPU FAN control
- Coin battery holder for RTC

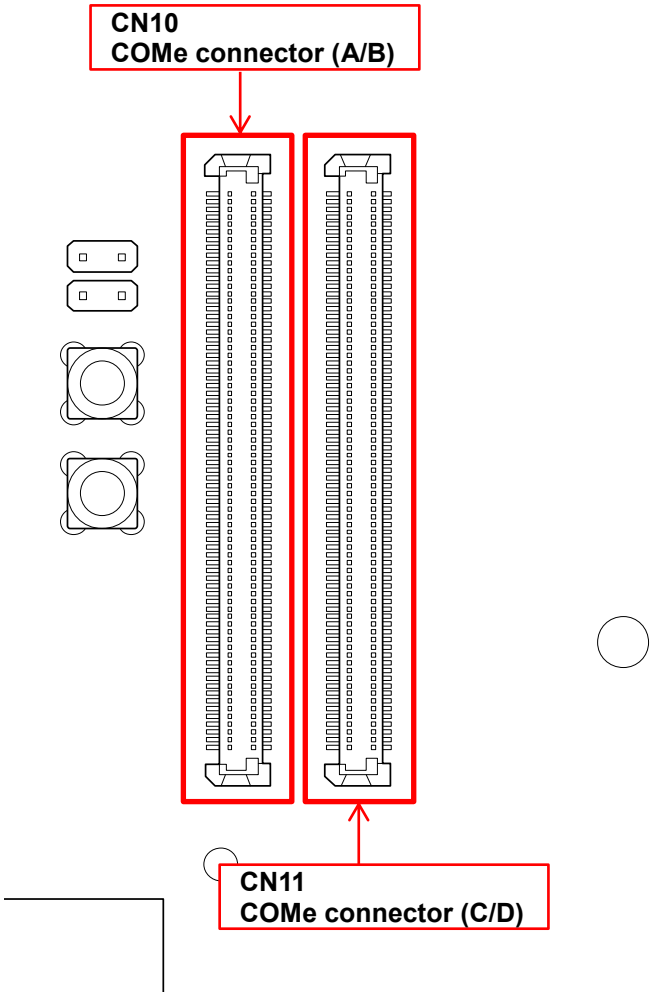

Figure 7.2.9-1 CN10 and CN11 (COMe Connectors)

7.3.1.COMe-LAN

The board's Gigabit Ethernet I/F of the COMe modules is connected to the 10/100/1000 Base-T compatible RJ-45 connector (CN12).

A block diagram of the area around the COMe connector and LAN connector is shown below.

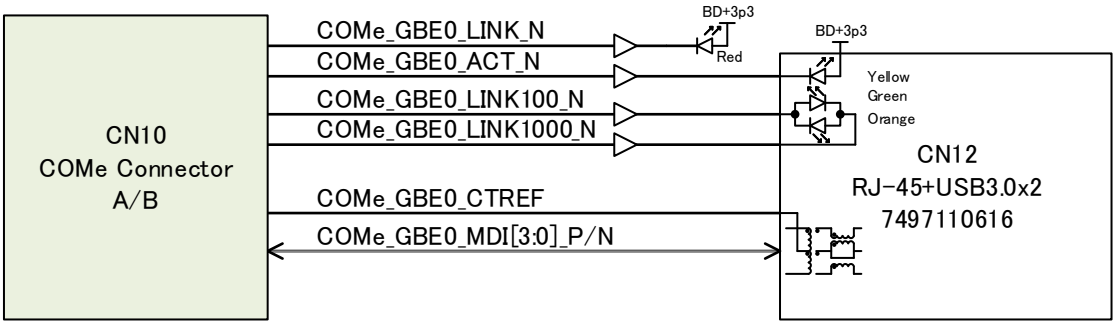

Figure 7.3.1-1 COMe-LAN Area Block Diagram

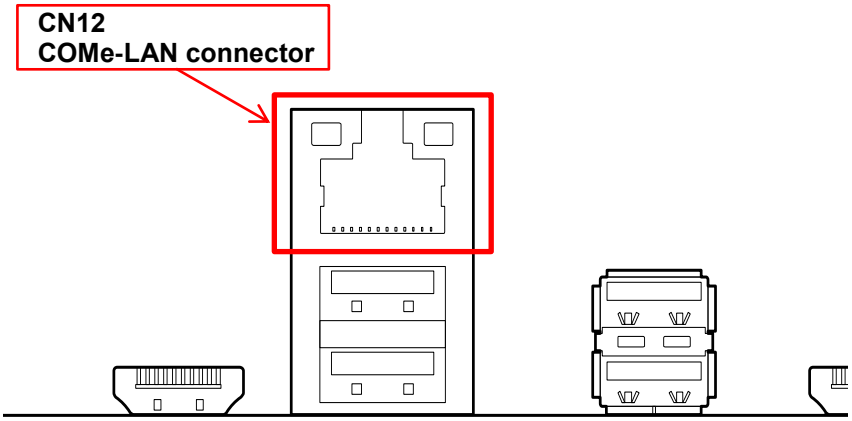

Figure 7.3.1-2 CN12 (COMe-LAN Connector)

7.3.2.HDMI Output (COMe)

The board is equipped with an HDMI Type-A connector (CN14) for image output from the COMe module.

Caution	The board is equipped with an HDMI output connector (CN6) for the FPGA, which is the same shape connector, so be careful when connecting to it.

A block diagram of the area around the COMe connector and HDMI output is shown below.

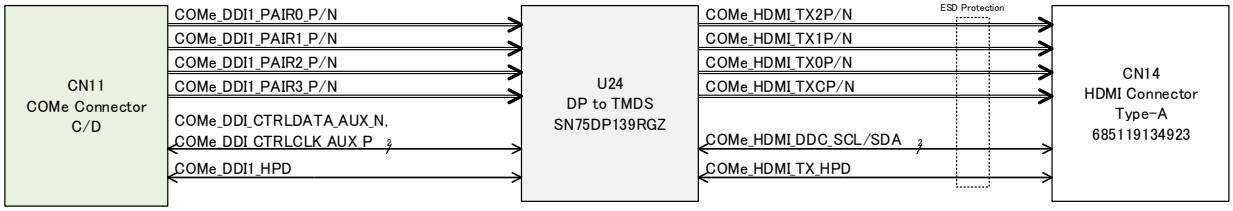

Figure 7.3.2-1 COMe-HDMI Output Area Block Diagram

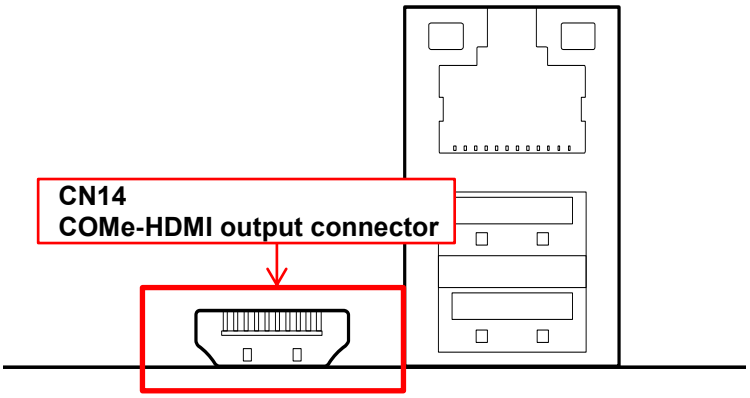

Figure 7.3.2-2 CN14 Installation

7.3.3.USB3.0

The board is equipped with 4 USB3.0 Type-A connectors (CN12 and CN13) for USB3.0 communications to the COMe module.

A block diagram of the area around the COMe connector and USB3.0 is shown below.

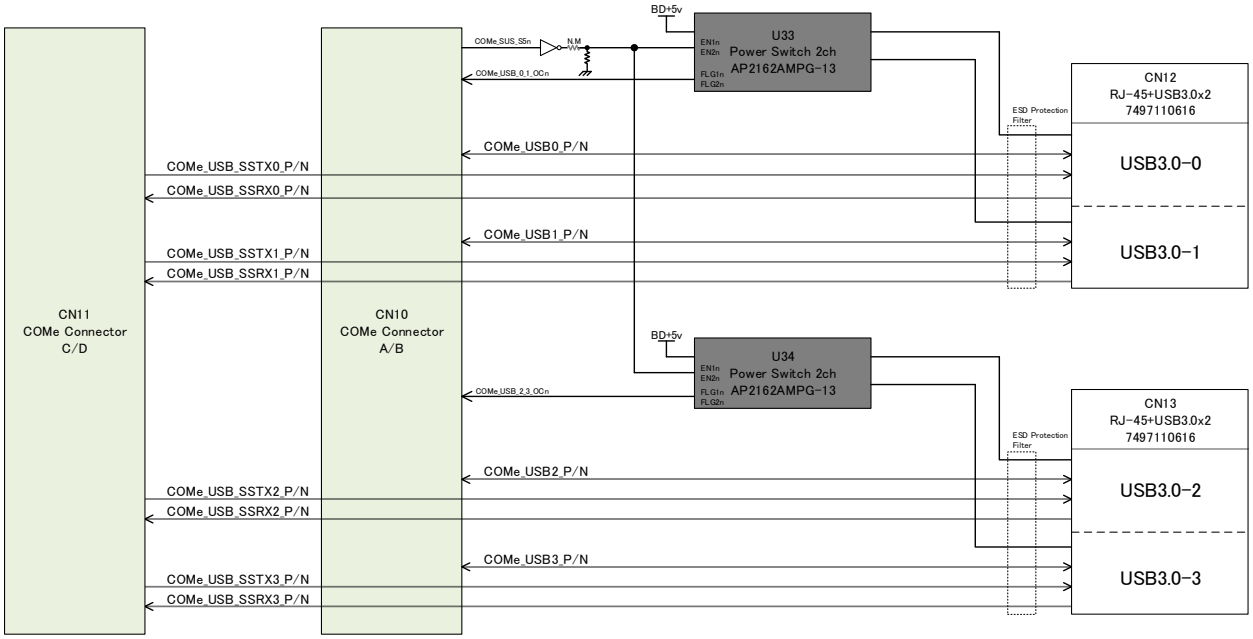

Figure 7.3.3-1 COMe-USB3.0 Area Block Diagram

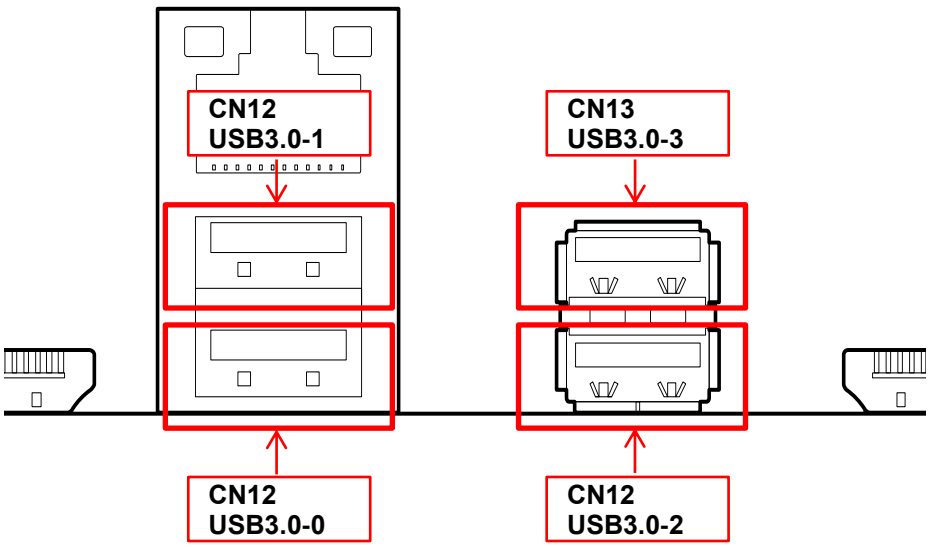

Figure 7.3.3-2 CN12 and CN13 (USB3.0)

7.3.4.SATA

The board is equipped with a connector (CN15) that integrates the SATA power supply and the connector for SATA signals for SATA communications to the COMe module. The SATA access lamp is an LED (LED11).

Caution	The SATA connector on the board is a female connector, so be careful of the orientation of the connector when connecting cables.

A block diagram of the area around the COMe connector and SATA connector is shown below.

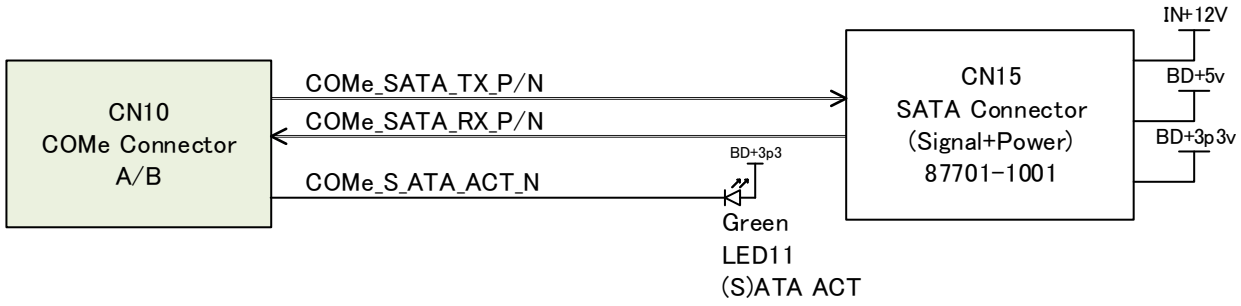

Figure 7.3.4-1 COMe-SATA Output Area Block Diagram

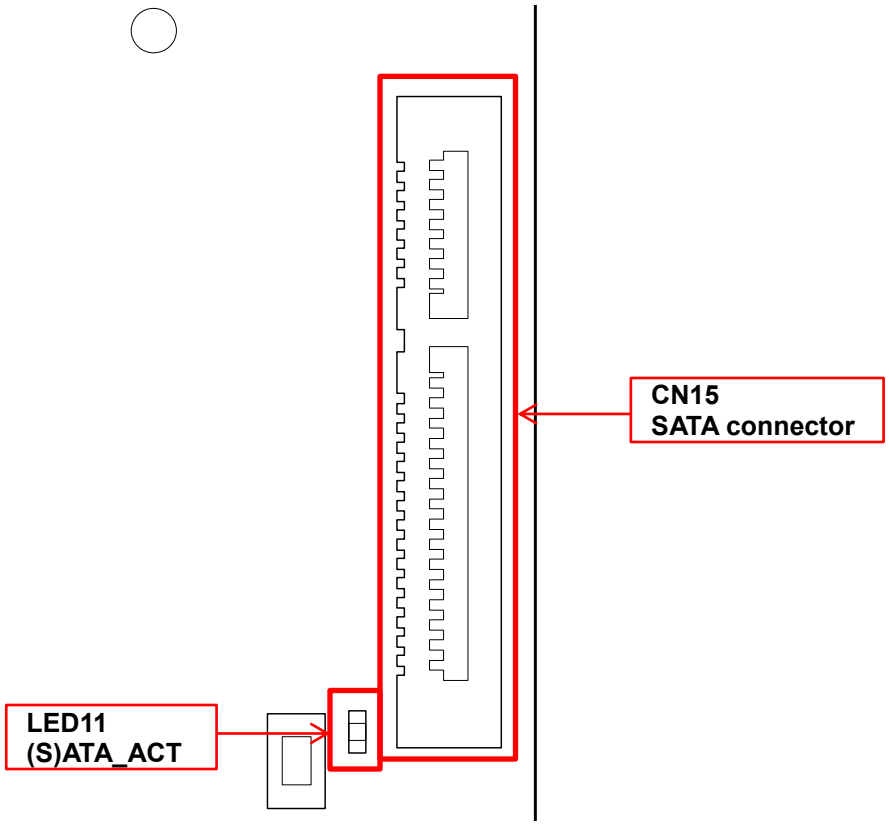

Figure 7.3.4-2 CN15 (SATA Connector)

7.3.5.CPU FAN

The board is equipped with a fan connector (CN22) for the COMe module. Connect the cooling fan for the COMe if needed.

A block diagram of the area around the COMe-FAN connector is shown below.

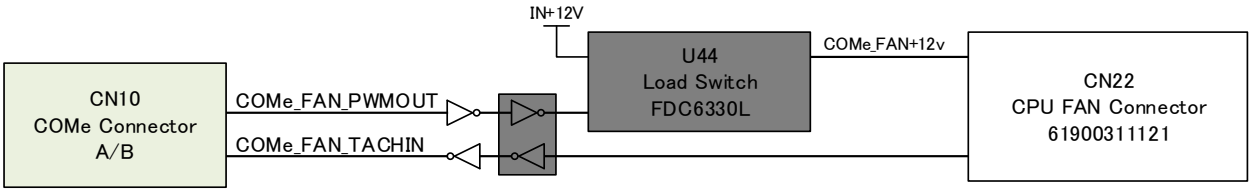

Figure 7.3.5-1 COMe-FAN Output Area Block Diagram

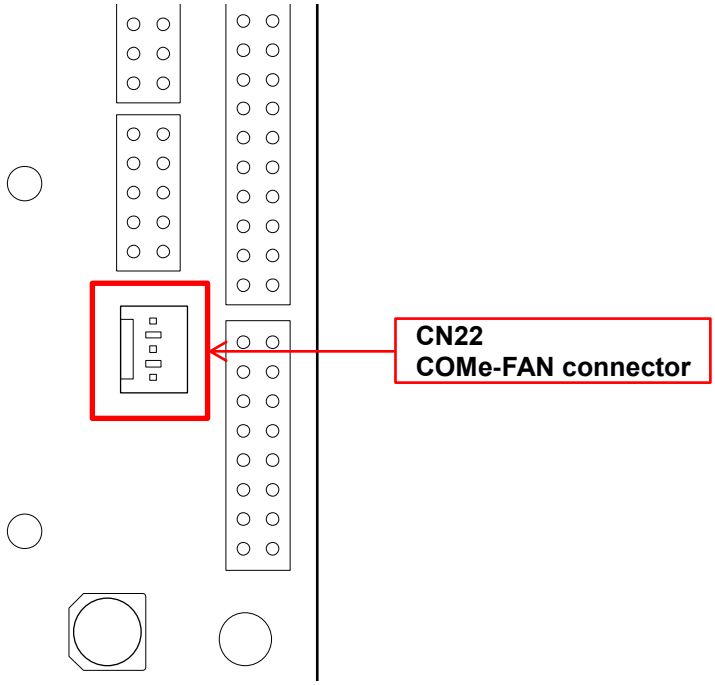

Figure 7.3.5-2 CN22 (FAN Connector for COMe)

7.3.6.Coin Battery Holder

The board is equipped with a coin battery holder (CN21) for the RTC on the COMe module. Insert a CR2030 size coin battery as needed.

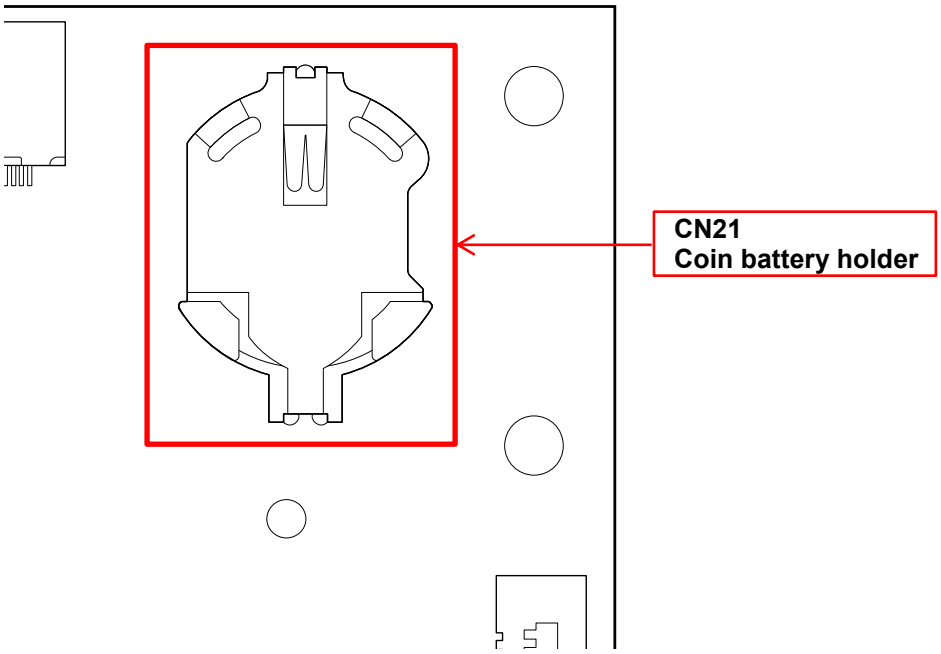

Figure 7.3.6-1 CN21 (Coin Battery Holder)

7.3.7.Reset Switch for COMe Module

The board is equipped with a push switch (SW9) for resetting the COMe module. Execute a reset if needed.
By pushing this switch, the COMe_SYS_RESET_N signal changes to L, and the COMe module is reset.

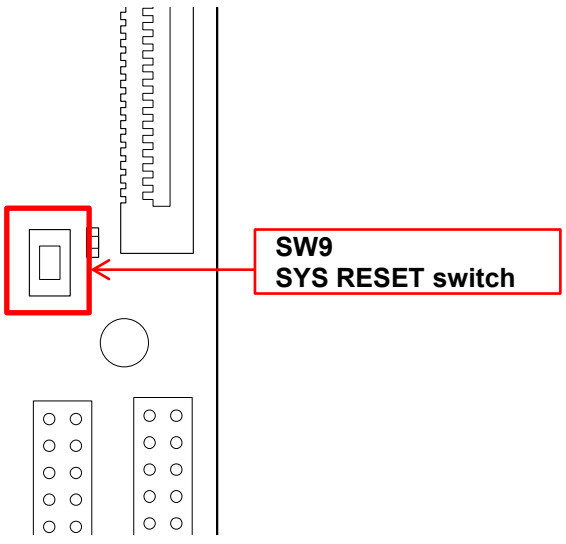

Figure 7.3.7-1 SW9 (COMe SYS RESET)

8. Document Revision History

Date	Revision	Changes
MAY 15, 2018	1.0	First edition