Hydra Schematic

Module Name	Rev.	Date of Issue	Document Number
Hydra Schematic	A	2013.9.6	S12-010

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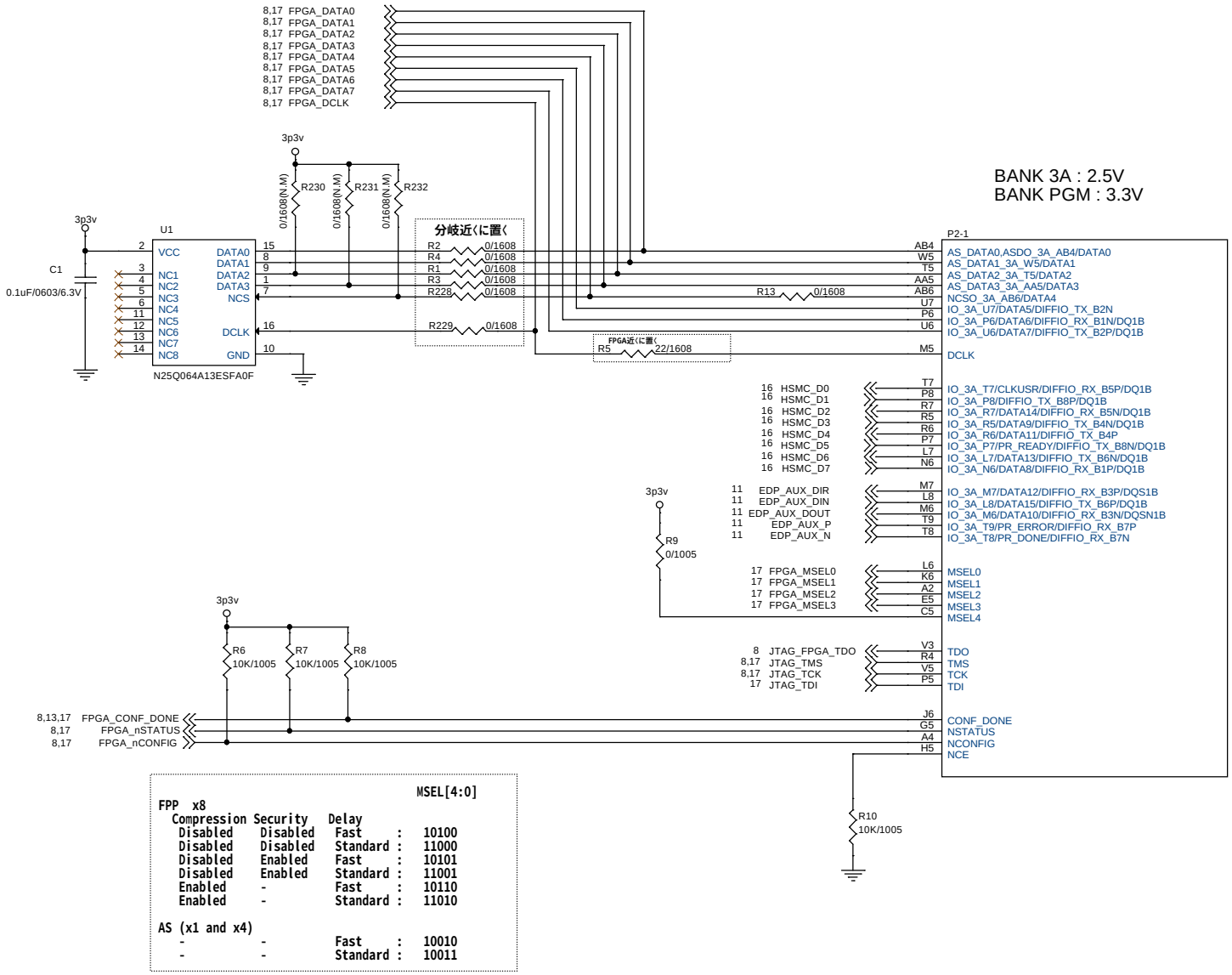

MSEL[4:0]				
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Disabled	Disabled	Standard	:	11000
Disabled	Enabled	Fast	:	10101
Disabled	Enabled	Standard	:	11001
Enabled	-	Fast	:	10110
Enabled	-	Standard	:	11010
AS (x1 and x4)				
-	-	Fast	:	10010
-	-	Standard	:	11011

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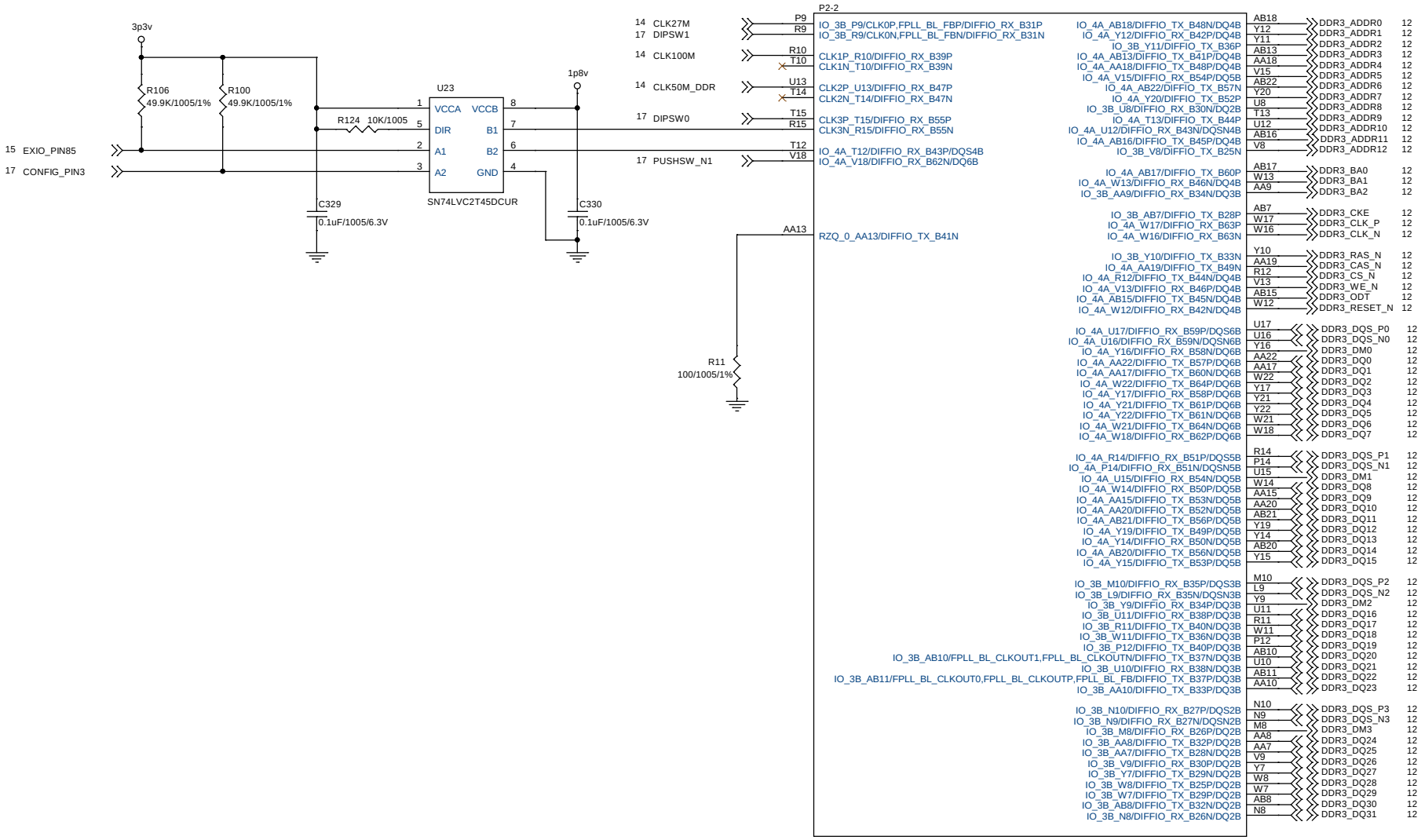
BANK 3B : 1.5V

BANK 4A : 1.5V



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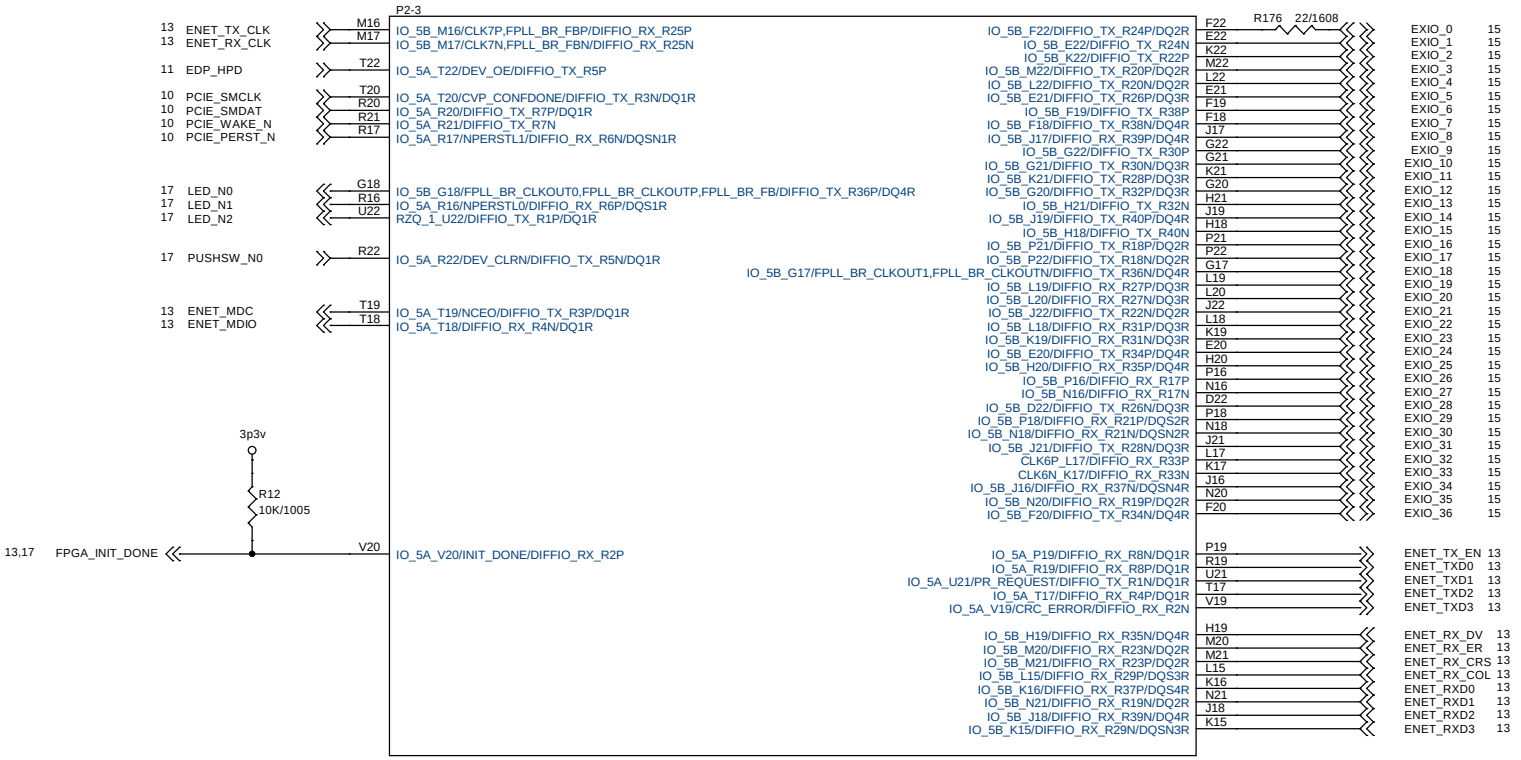
BANK 5A : 3.3V
BANK 5B : 2.5V or 3.3V



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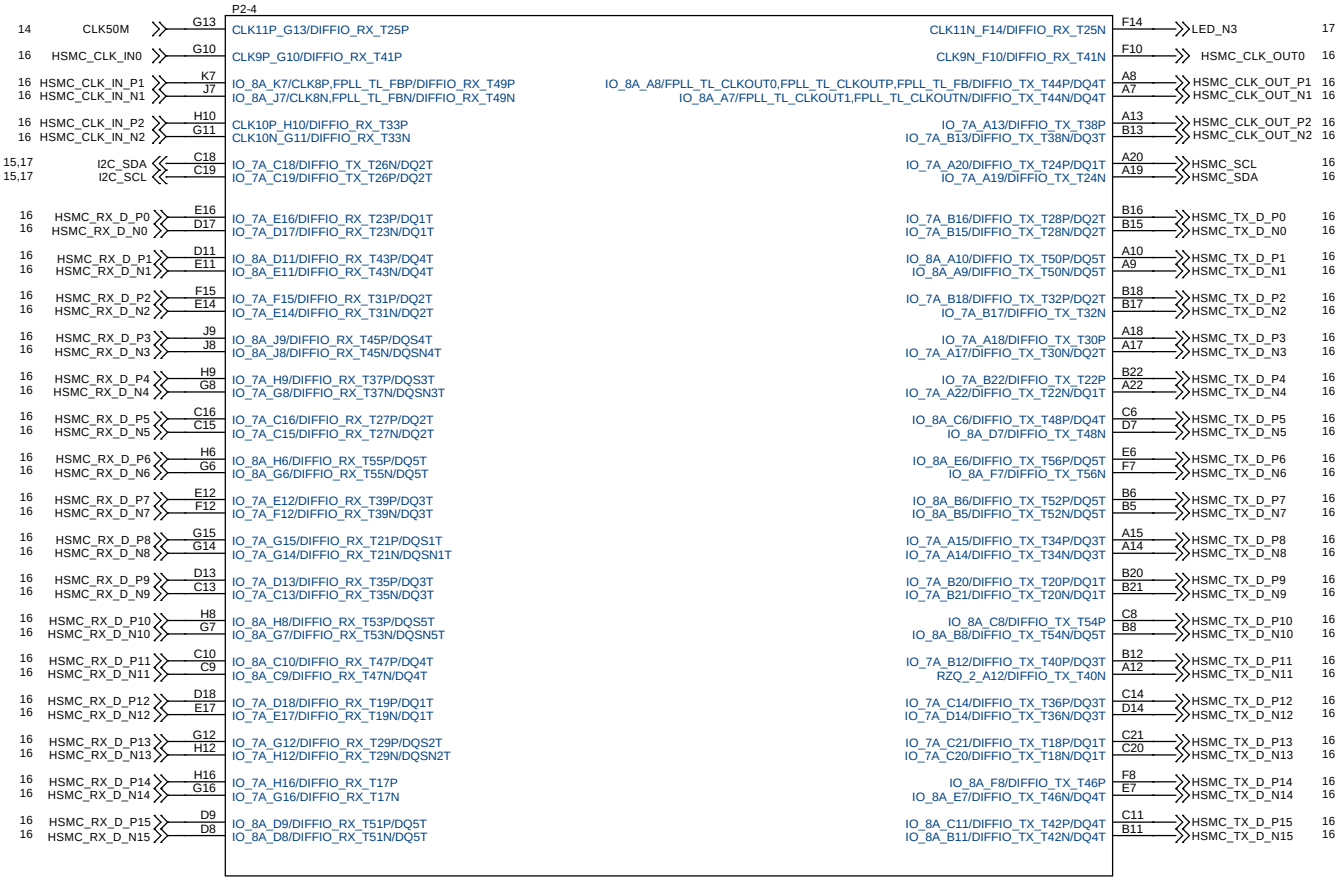
BANK 7A : 2.5V
BANK 8A : 2.5V



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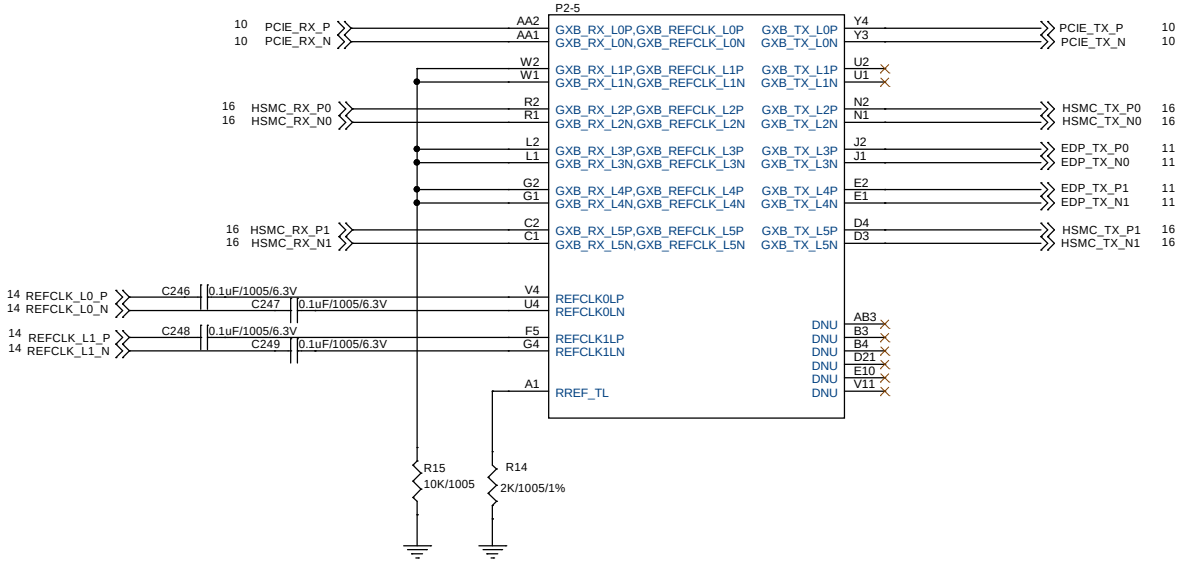

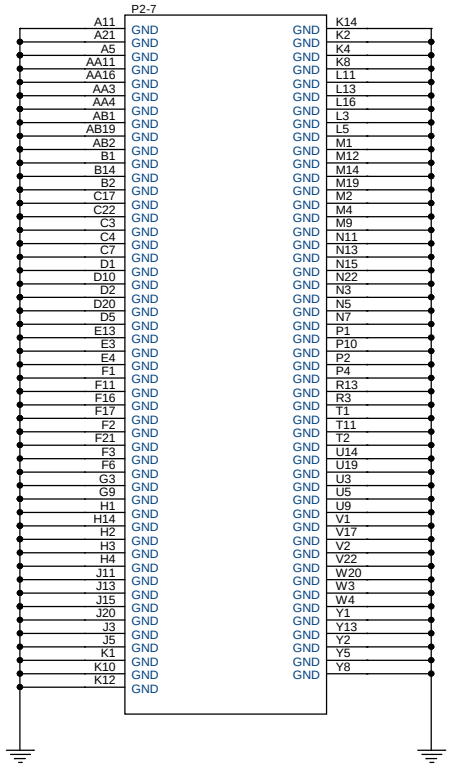

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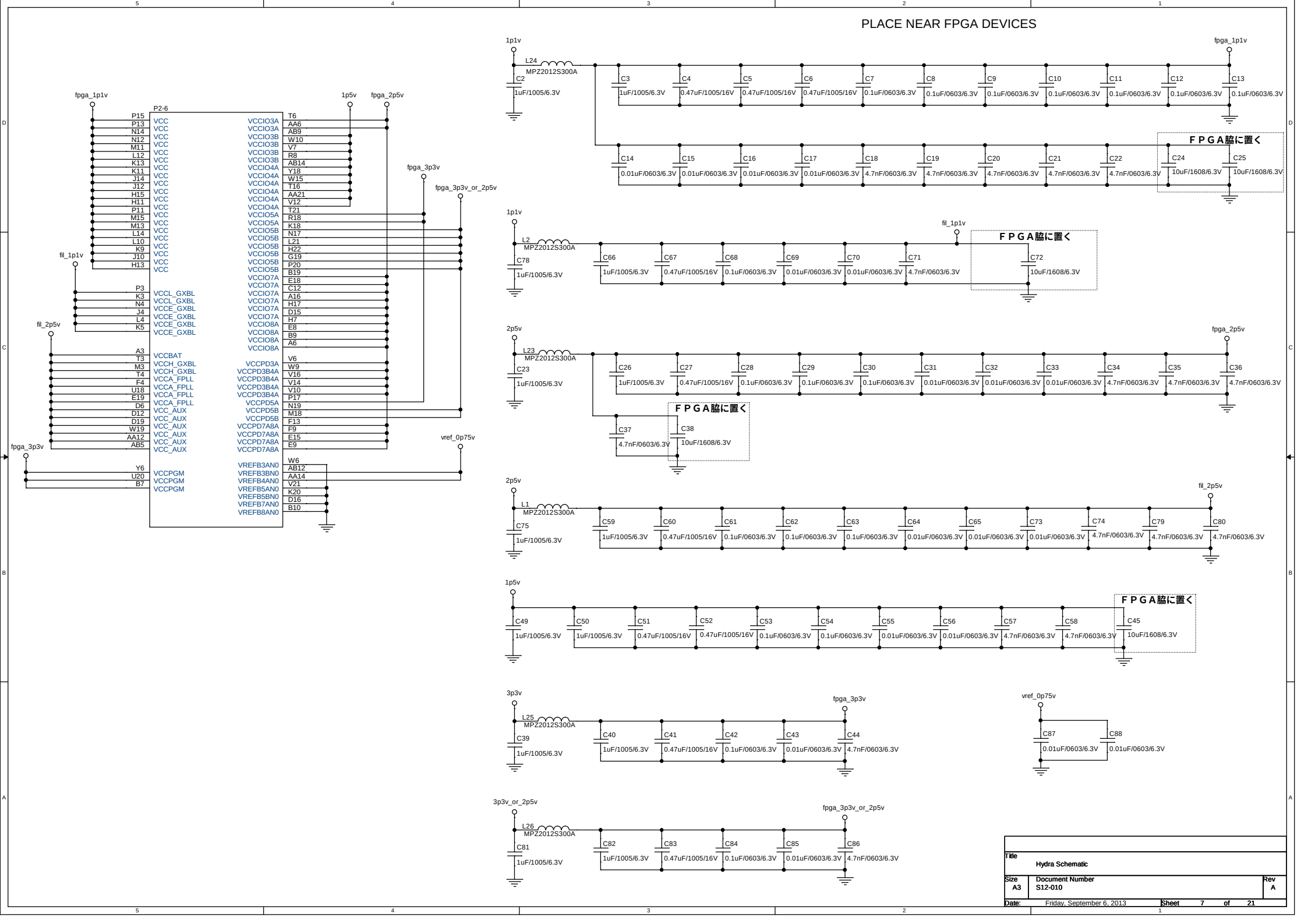

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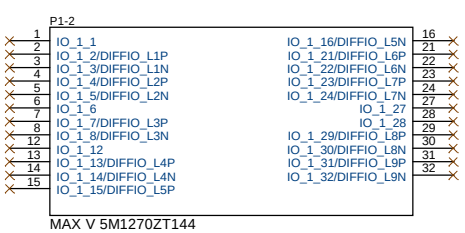

MAX V 5M1270ZT144
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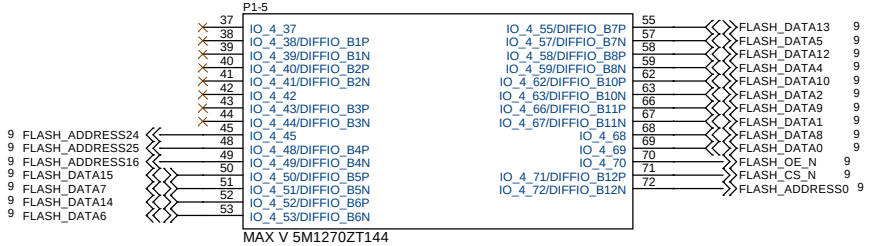

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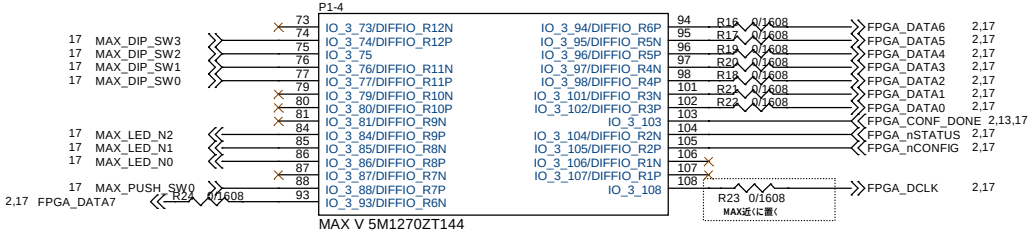

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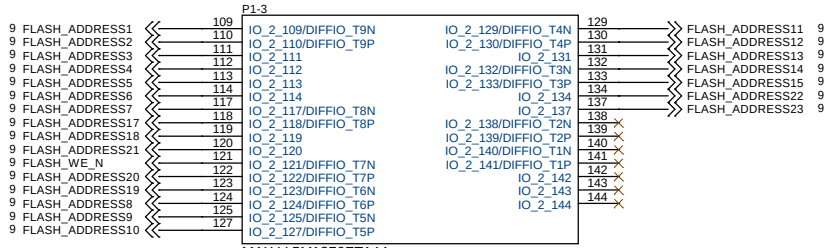

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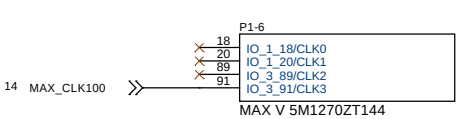

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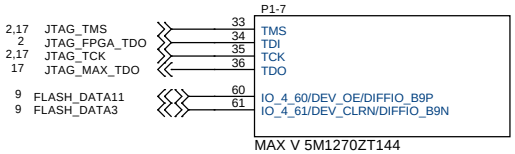

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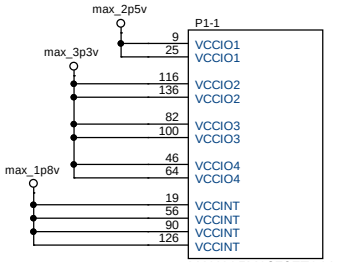

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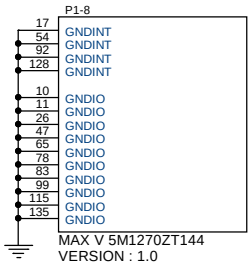

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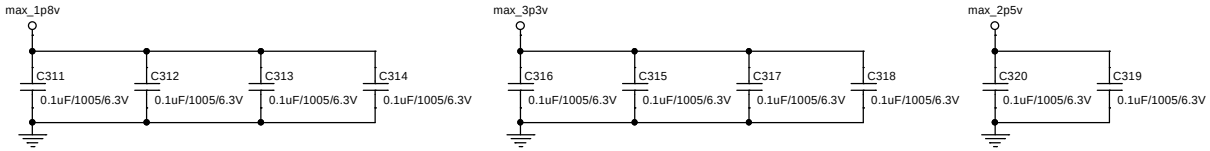

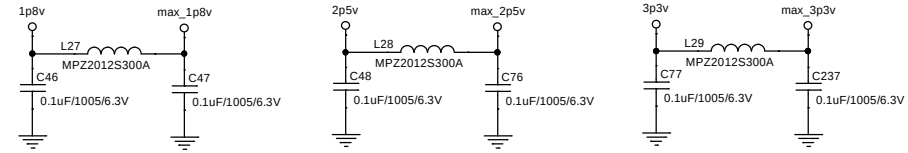

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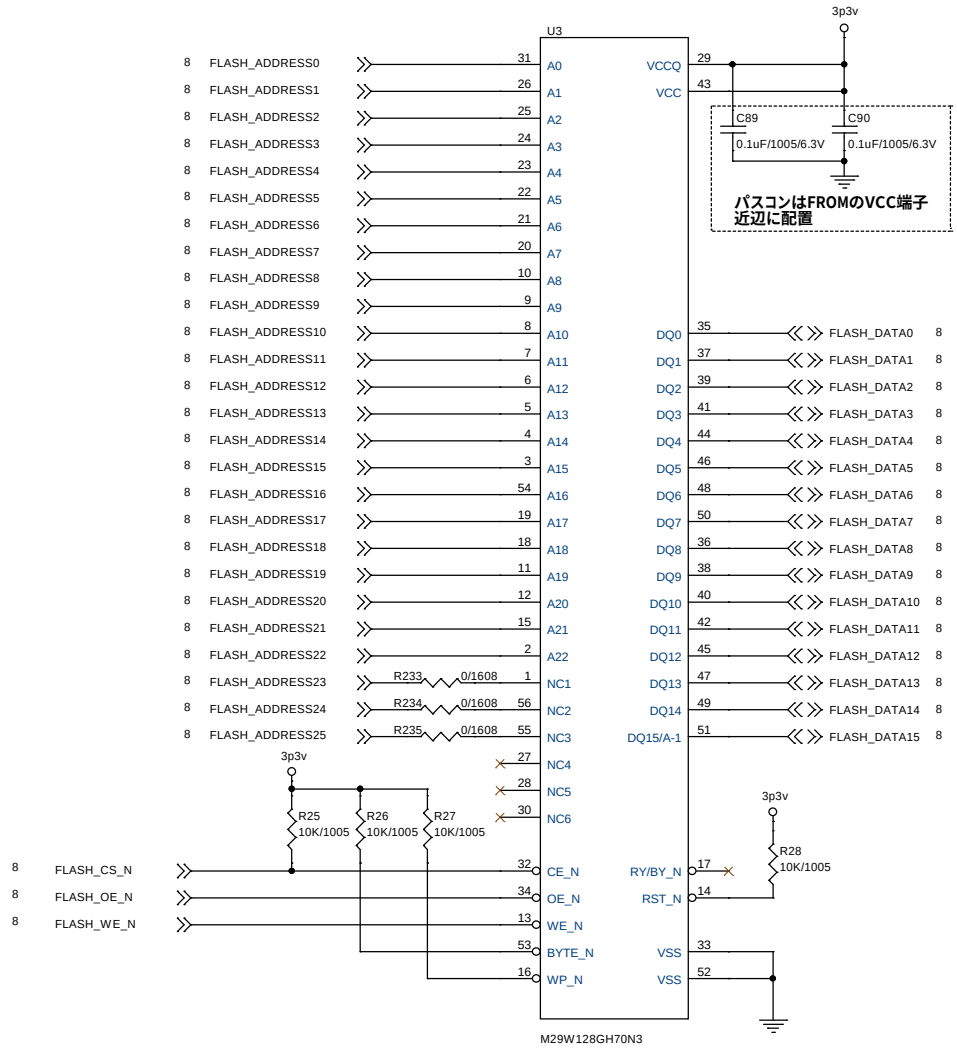

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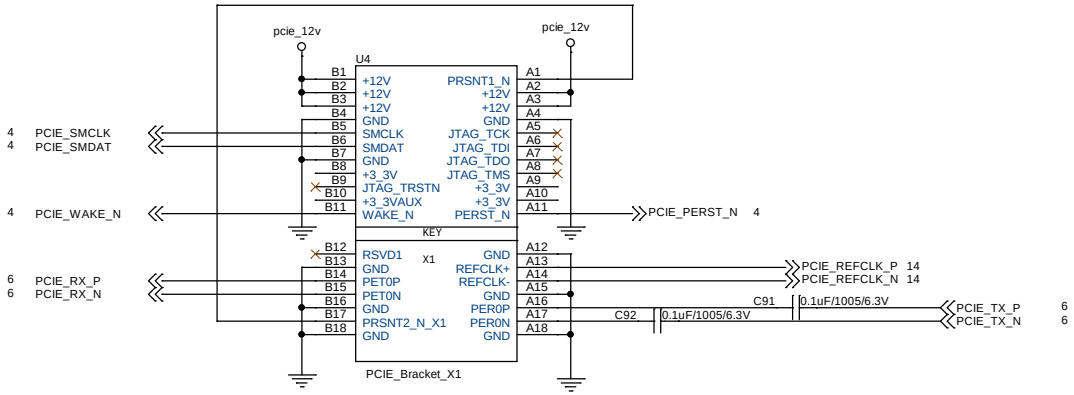

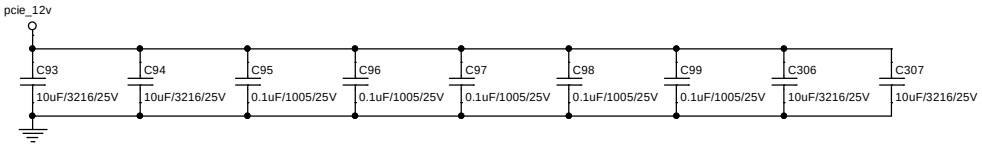

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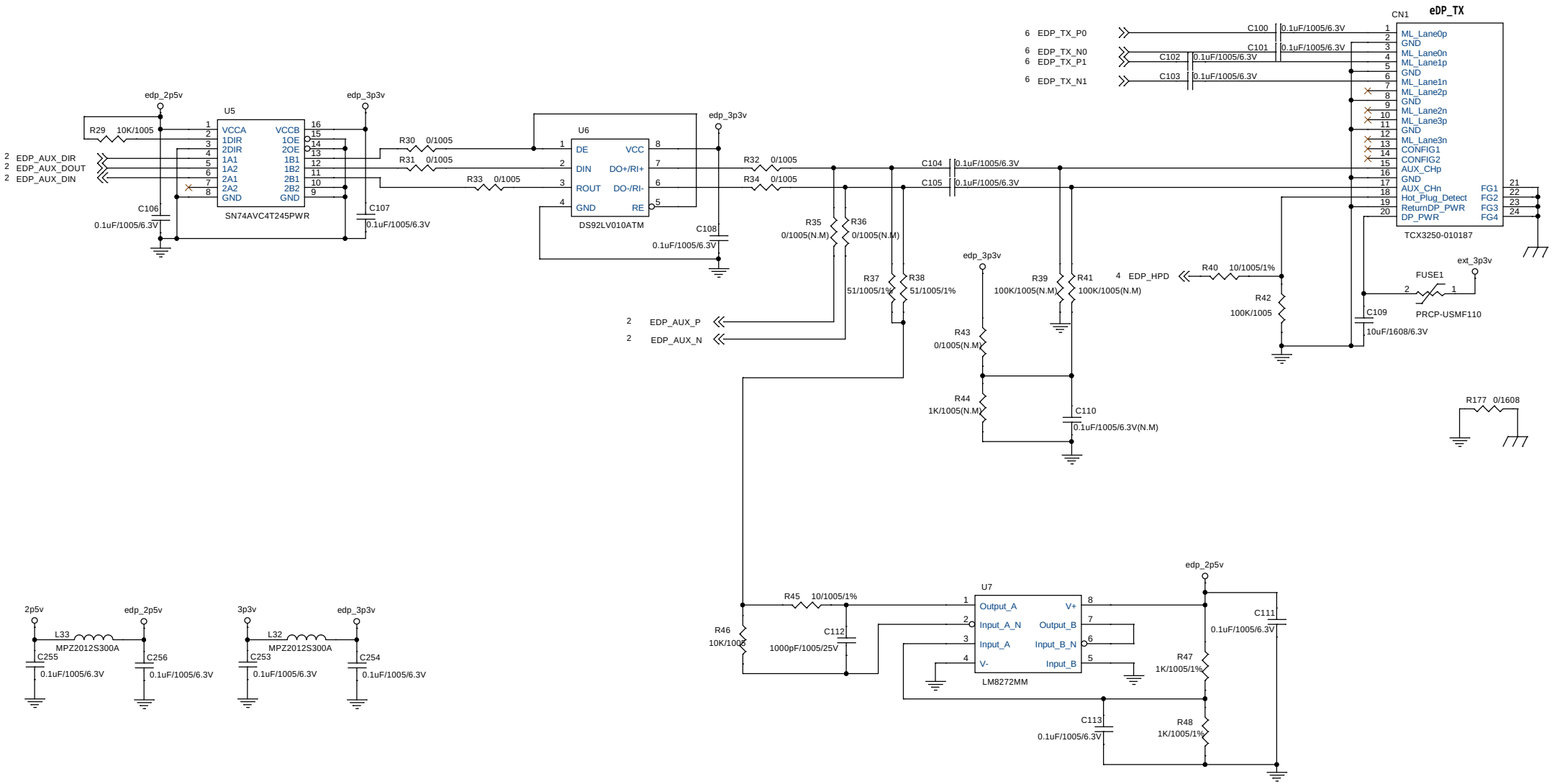

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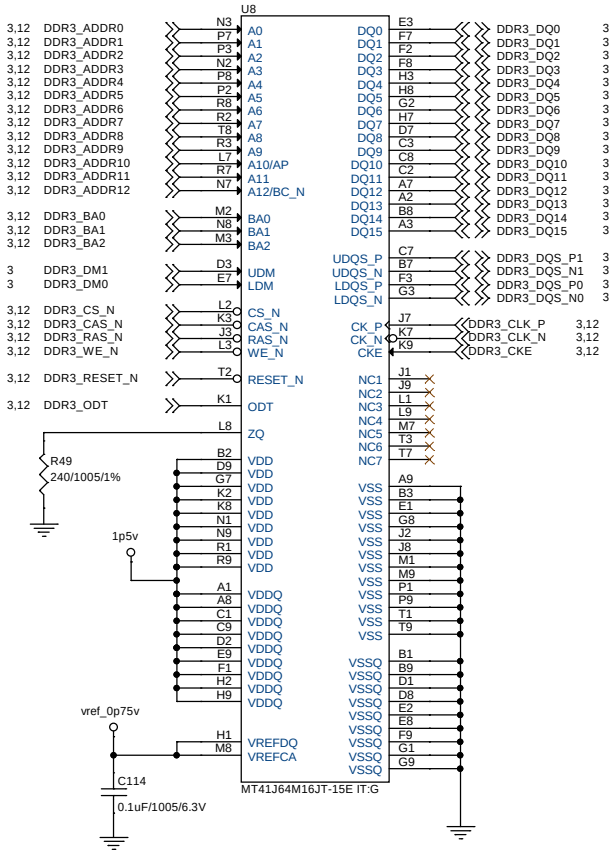

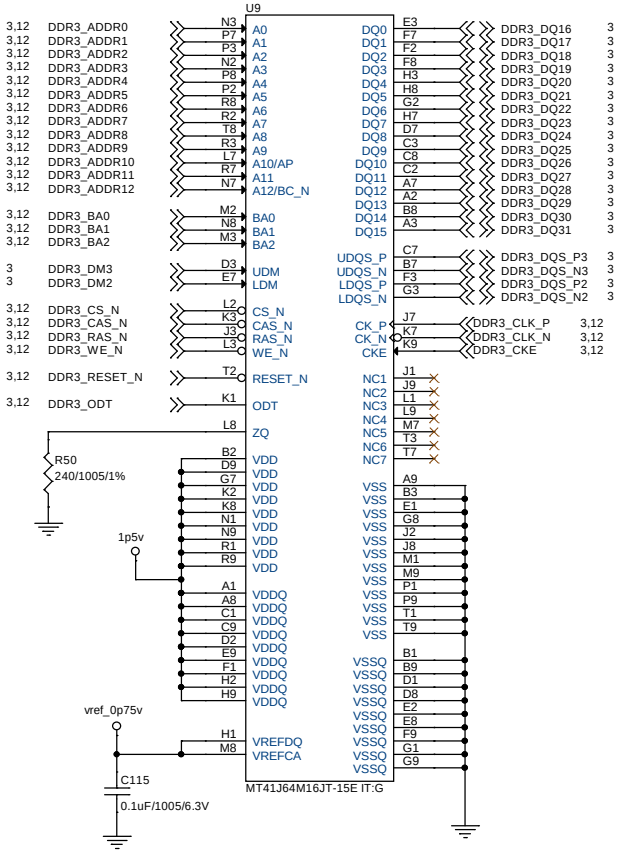

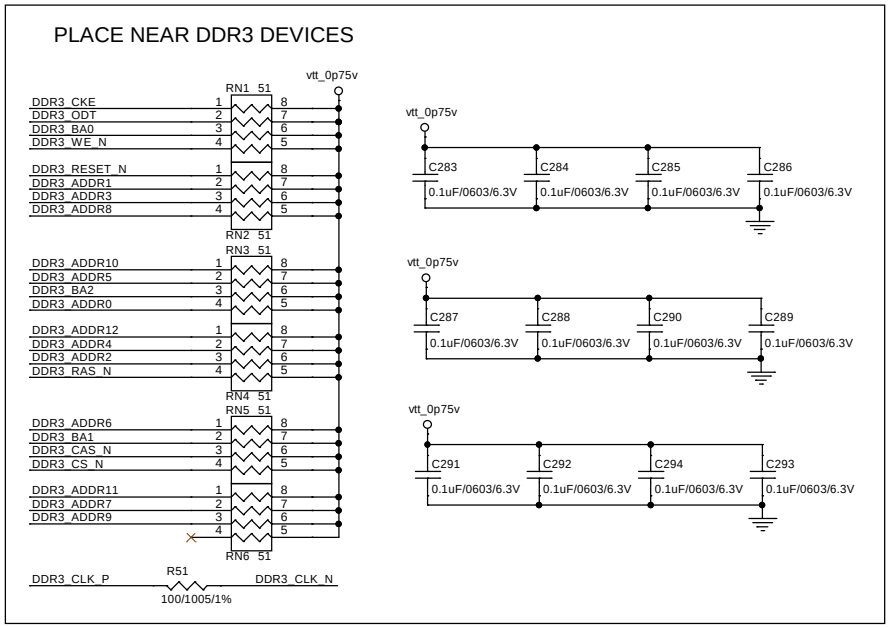

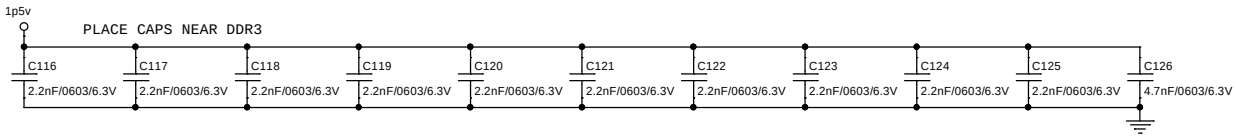

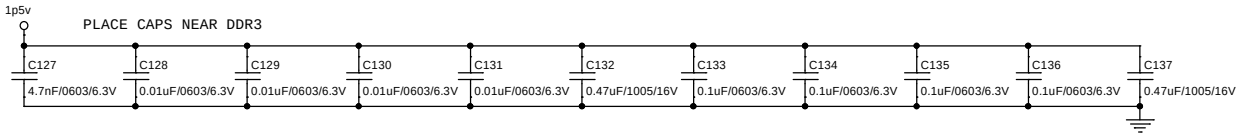

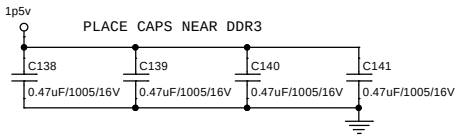

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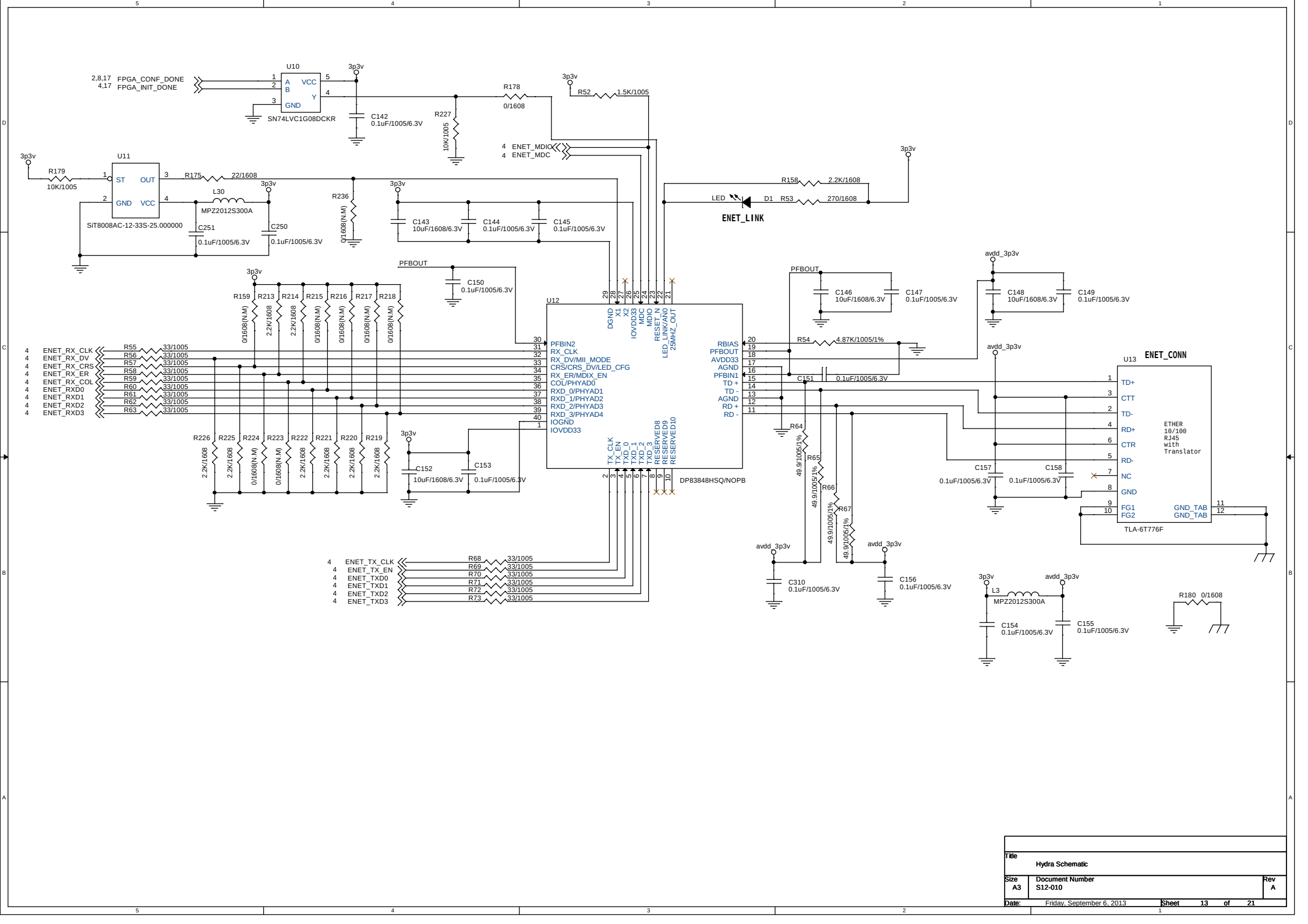
2,8,17 FPGA_CONF_DONE
4,17 FPGA_INIT_DONE
U10
SN74LVC1G08DCKR
C142 0.1uF/1005/6.3V
R227 10K/1005
R178 0/1608
R52 1.5K/1005
4 ENET_MDIO
4 ENET_MDC
U11
SiT8008AC-12-33S-25.000000
R179 10K/1005
R175 22/1608
L30 MPZ2012S300A
C251 0.1uF/1005/6.3V
C250 0.1uF/1005/6.3V
R236 0/1608(N.M)
C143 10uF/1608/6.3V
C144 0.1uF/1005/6.3V
C145 0.1uF/1005/6.3V
R158 2.2K/1608
LED
D1
R53 270/1608
ENET_LINK
PFBOUT
C150 0.1uF/1005/6.3V
R159 0/1608(N.M)
R213 2.2K/1608
R214 2.2K/1608
R215 0/1608(N.M)
R216 0/1608(N.M)
R217 0/1608(N.M)
R218 0/1608(N.M)
U12
DP83848HSQ/NOPB
4 ENET_RX_CLK
4 ENET_RX_DV
4 ENET_RX_CRS
4 ENET_RX_ER
4 ENET_RX_COL
4 ENET_RXD0
4 ENET_RXD1
4 ENET_RXD2
4 ENET_RXD3
R55 33/1005
R56 33/1005
R57 33/1005
R58 33/1005
R59 33/1005
R60 33/1005
R61 33/1005
R62 33/1005
R63 33/1005
R226 2.2K/1608
R225 2.2K/1608
R224 0/1608(N.M)
R223 0/1608(N.M)
R222 2.2K/1608
R221 2.2K/1608
R220 2.2K/1608
R219 2.2K/1608
C152 10uF/1608/6.3V
C153 0.1uF/1005/6.3V
4 ENET_TX_CLK
4 ENET_TX_EN
4 ENET_TXD0
4 ENET_TXD1
4 ENET_TXD2
4 ENET_TXD3
R68 33/1005
R69 33/1005
R70 33/1005
R71 33/1005
R72 33/1005
R73 33/1005
avdd_3p3v
C146 10uF/1608/6.3V
C147 0.1uF/1005/6.3V
C148 10uF/1608/6.3V
C149 0.1uF/1005/6.3V
R54 4.87K/1005/1%
C151 0.1uF/1005/6.3V
R64 49.9/1005/1%
R65 49.9/1005/1%
R66 49.9/1005/1%
R67 49.9/1005/1%
C310 0.1uF/1005/6.3V
C156 0.1uF/1005/6.3V
C157 0.1uF/1005/6.3V
C158 0.1uF/1005/6.3V
U13
ENET_CONN
ETHER 10/100 RJ45 with Translator
TLA-6T776F
L3 MPZ2012S300A
C154 0.1uF/1005/6.3V
C155 0.1uF/1005/6.3V
R180 0/1608
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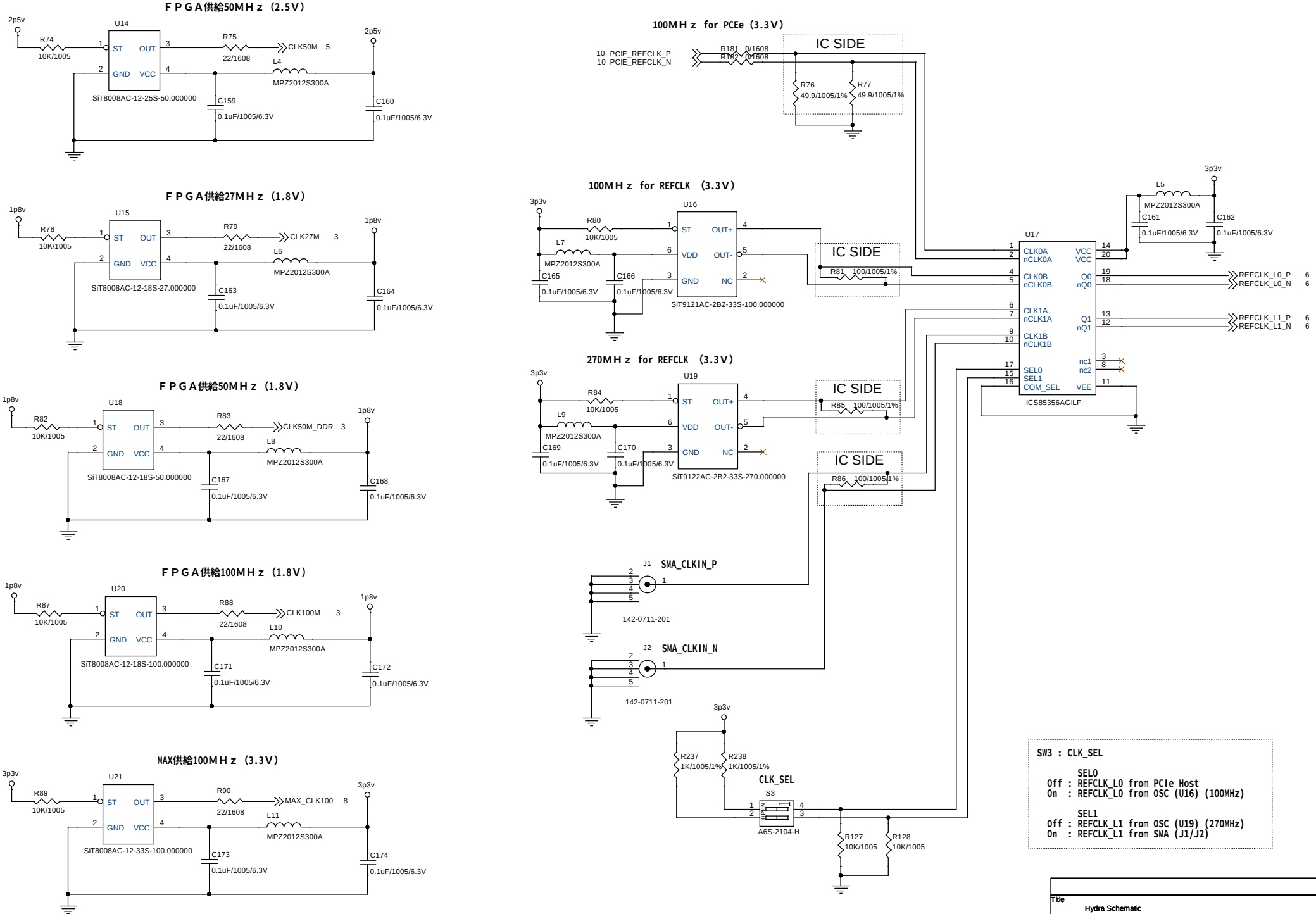

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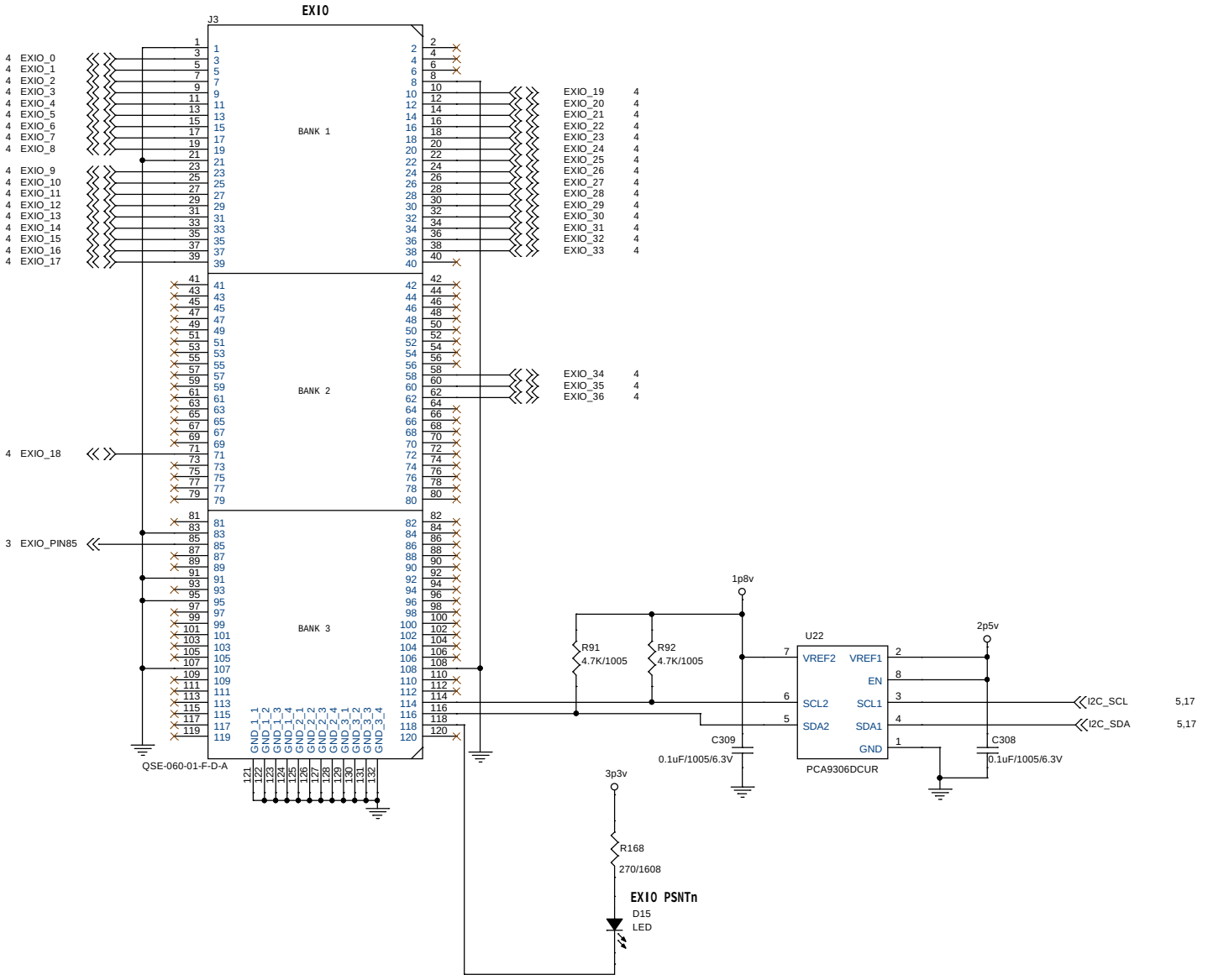

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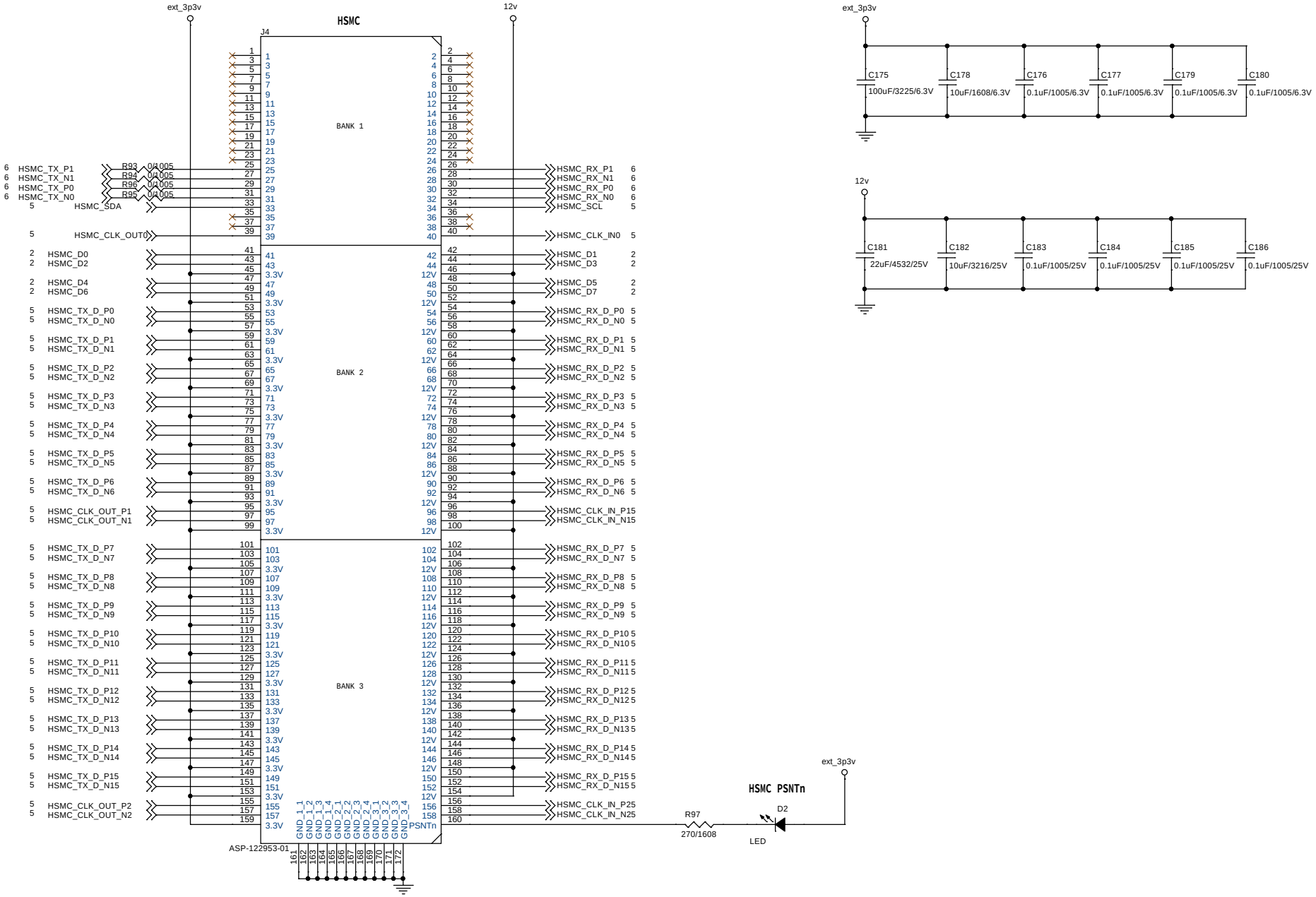

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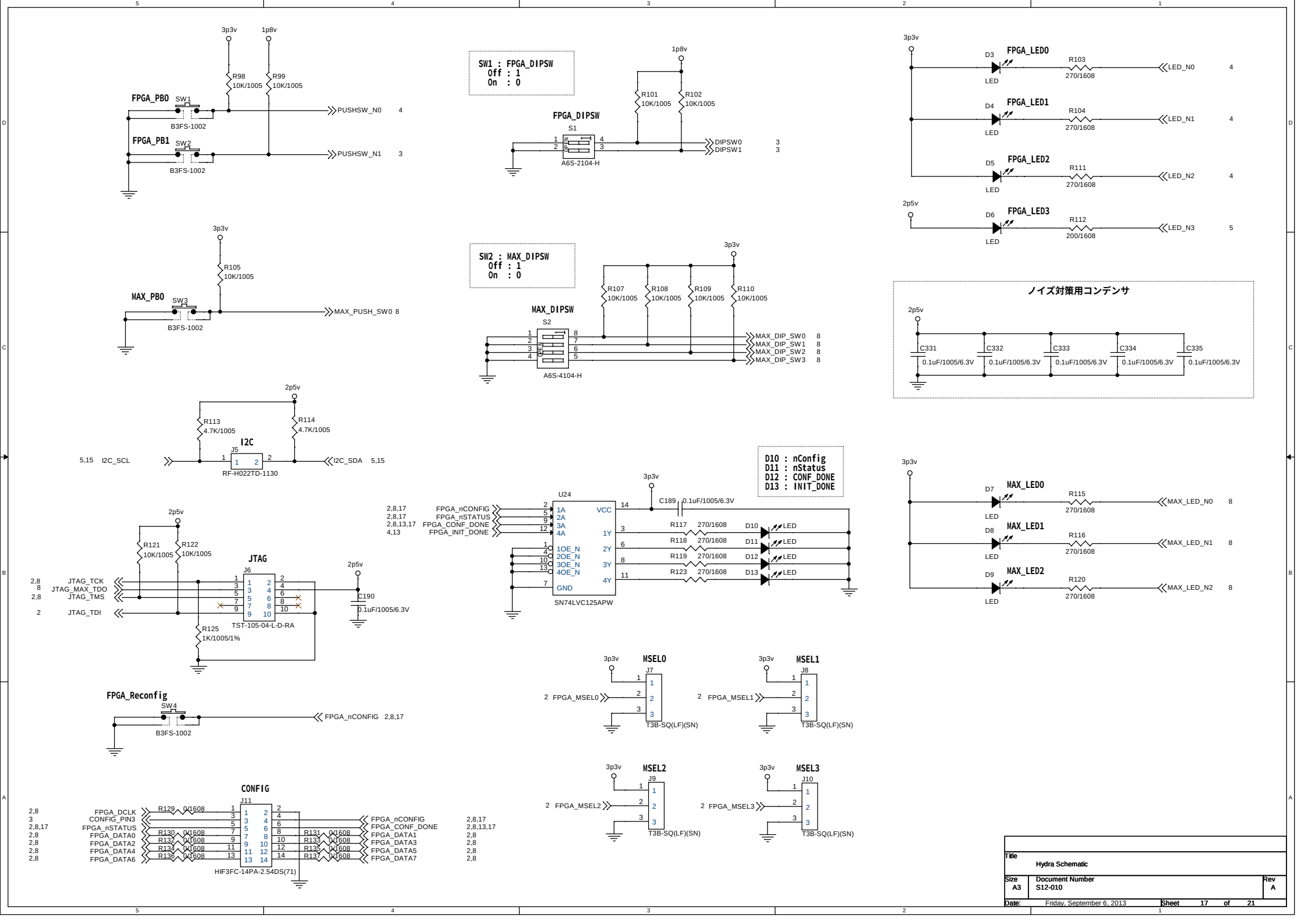
3p3v
1p8v
R98 10K/1005
R99 10K/1005
FPGA_PB0
SW1
B3FS-1002
PUSHSW_N0 4
FPGA_PB1
SW2
B3FS-1002
PUSHSW_N1 3
SW1 : FPGA_DIPSW
Off : 1
On : 0
R101 10K/1005
R102 10K/1005
FPGA_DIPSW
S1
A6S-2104-H
DIPSW0 3
DIPSW1 3
FPGA_LED0
D3
LED
R103 270/1608
LED_N0 4
FPGA_LED1
D4
R104 270/1608
LED_N1 4
FPGA_LED2
D5
R111 270/1608
LED_N2 4
2p5v
FPGA_LED3
D6
R112 200/1608
LED_N3 5
R105 10K/1005
MAX_PB0
SW3
B3FS-1002
MAX_PUSH_SW0 8
SW2 : MAX_DIPSW
Off : 1
On : 0
R107 10K/1005
R108 10K/1005
R109 10K/1005
R110 10K/1005
MAX_DIPSW
S2
A6S-4104-H
MAX_DIP_SW0 8
MAX_DIP_SW1 8
MAX_DIP_SW2 8
MAX_DIP_SW3 8
ノイズ対策用コンデンサ
C331 0.1uF/1005/6.3V
C332 0.1uF/1005/6.3V
C333 0.1uF/1005/6.3V
C334 0.1uF/1005/6.3V
C335 0.1uF/1005/6.3V
R113 4.7K/1005
R114 4.7K/1005
I2C
J5
RF-H022TD-1130
5,15 I2C_SCL
I2C_SDA 5,15
D10 : nConfig
D11 : nStatus
D12 : CONF_DONE
D13 : INIT_DONE
U24
SN74LVC125APW
2,8,17 FPGA_nCONFIG
2,8,17 FPGA_nSTATUS
2,8,13,17 FPGA_CONF_DONE
4,13 FPGA_INIT_DONE
C189 0.1uF/1005/6.3V
R117 270/1608
R118 270/1608
R119 270/1608
R123 270/1608
D10 LED
D11 LED
D12 LED
D13 LED
MAX_LED0
D7
R115 270/1608
MAX_LED_N0 8
MAX_LED1
D8
R116 270/1608
MAX_LED_N1 8
MAX_LED2
D9
R120 270/1608
MAX_LED_N2 8
R121 10K/1005
R122 10K/1005
JTAG
J6
2,8 JTAG_TCK
8 JTAG_MAX_TDO
2,8 JTAG_TMS
2 JTAG_TDI
C190 0.1uF/1005/6.3V
R125 1K/1005/1%
TST-105-04-L-D-RA
FPGA_Reconfig
SW4
B3FS-1002
FPGA_nCONFIG 2,8,17
MSEL0
J7
2 FPGA_MSEL0
T3B-SQ(LF)(SN)
MSEL1
J8
2 FPGA_MSEL1
MSEL2
J9
2 FPGA_MSEL2
MSEL3
J10
2 FPGA_MSEL3
CONFIG
J11
HIF3FC-14PA-2.54DS(71)
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3 CONFIG_PIN3
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2,8 FPGA_DATA0
2,8 FPGA_DATA2
2,8 FPGA_DATA4
2,8 FPGA_DATA6
R129 0/1608
R130 0/1608
R132 0/1608
R134 0/1608
R136 0/1608
R131 0/1608
R133 0/1608
R135 0/1608
R137 0/1608
FPGA_nCONFIG 2,8,17
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FPGA_DATA1 2,8
FPGA_DATA3 2,8
FPGA_DATA5 2,8
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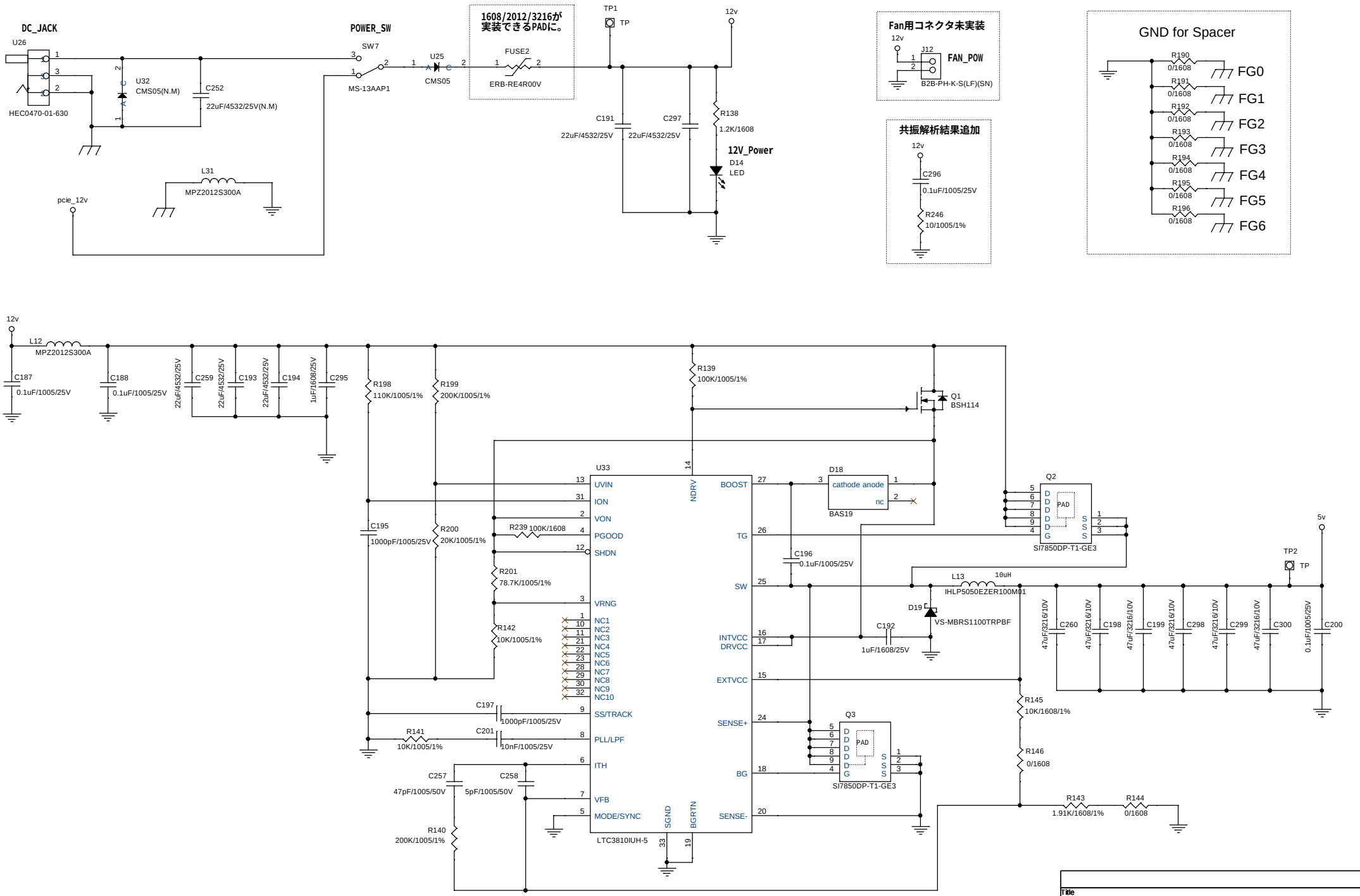

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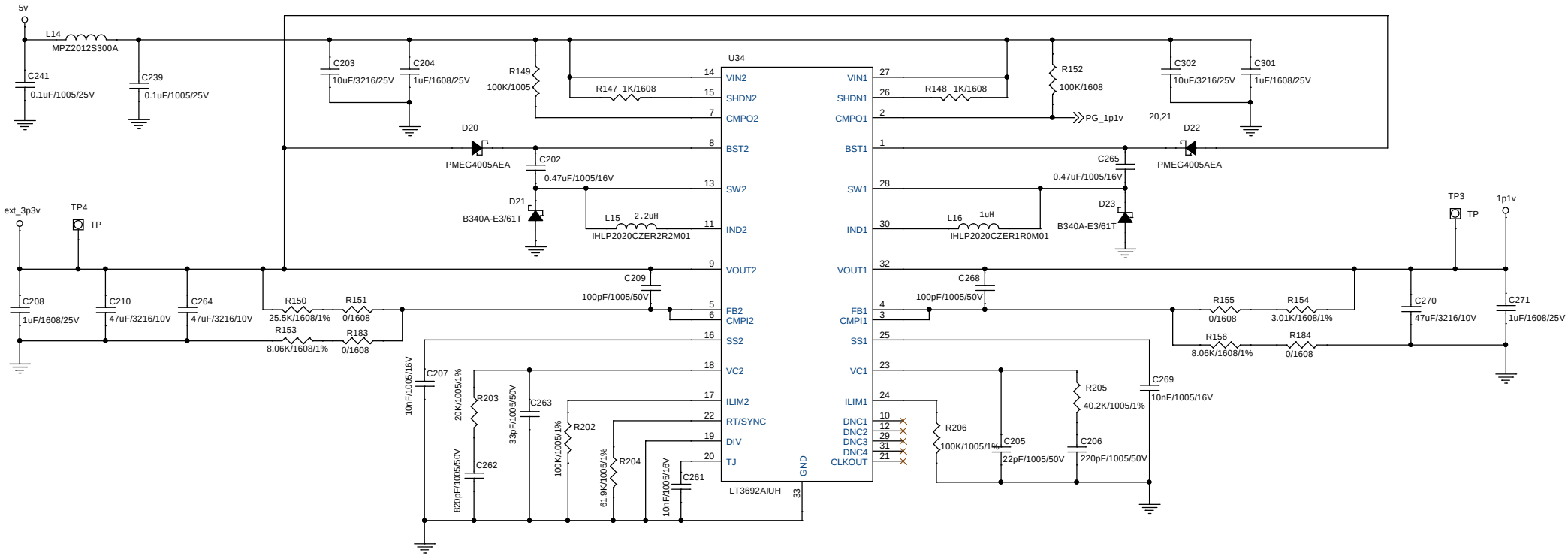
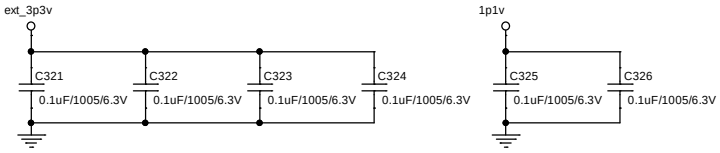
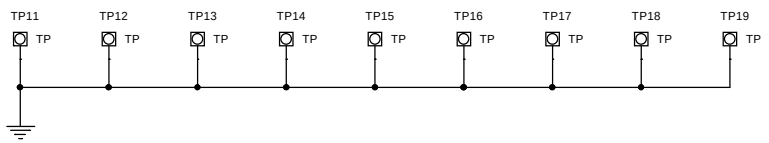


共振解析結果追加



GND Test Point



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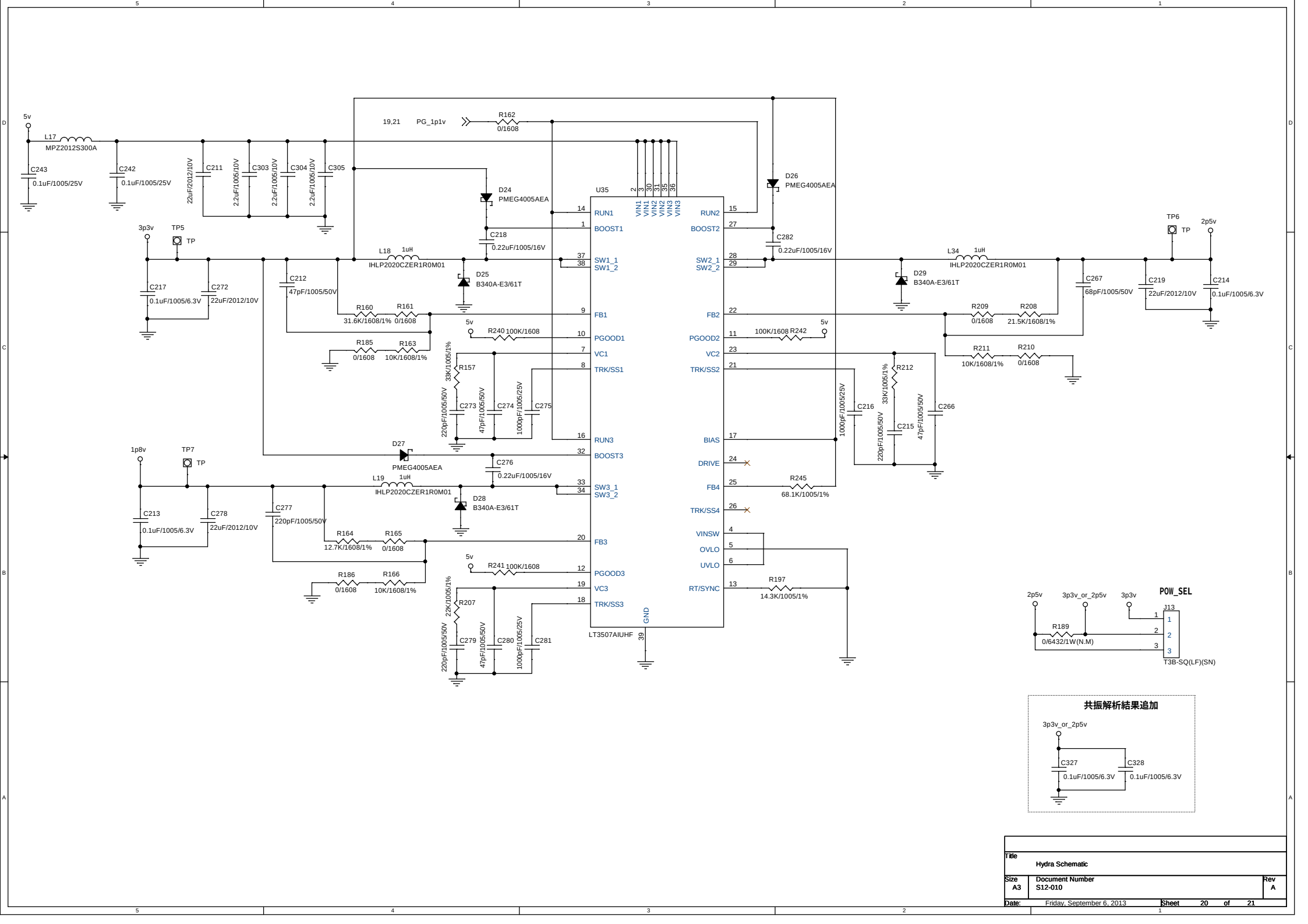
5v
L17
MPZ2012S300A
C243
0.1uF/1005/25V
C242
0.1uF/1005/25V
22uF/2012/10V
C211
2.2uF/1005/10V
C303
2.2uF/1005/10V
C304
2.2uF/1005/10V
C305
19,21
PG_1p1v
R162
0/1608
D24
PMEG4005AEA
D26
PMEG4005AEA
U35
VIN1
VIN1
VIN2
VIN2
VIN3
VIN3
RUN1
BOOST1
SW1_1
SW1_2
FB1
PGOOD1
VC1
TRK/SS1
RUN3
BOOST3
SW3_1
SW3_2
FB3
PGOOD3
VC3
TRK/SS3
RUN2
BOOST2
SW2_1
SW2_2
FB2
PGOOD2
VC2
TRK/SS2
BIAS
DRIVE
FB4
TRK/SS4
VINSW
OVLO
UVLO
RT/SYNC
GND
LT3507AIUHF
3p3v
TP5
TP
C217
0.1uF/1005/6.3V
C272
22uF/2012/10V
L18
1uH
IHLP2020CZER1R0M01
C218
0.22uF/1005/16V
D25
B340A-E3/61T
C212
47pF/1005/50V
R160
31.6K/1608/1%
R161
0/1608
R185
0/1608
R163
10K/1608/1%
5v
R240
100K/1608
R157
33K/1005/1%
C273
220pF/1005/50V
C274
47pF/1005/50V
C275
1000pF/1005/25V
1p8v
TP7
TP
C213
0.1uF/1005/6.3V
C278
22uF/2012/10V
D27
PMEG4005AEA
C276
0.22uF/1005/16V
L19
1uH
IHLP2020CZER1R0M01
D28
B340A-E3/61T
C277
220pF/1005/50V
R164
12.7K/1608/1%
R165
0/1608
R186
0/1608
R166
10K/1608/1%
5v
R241
100K/1608
R207
22K/1005/1%
C279
220pF/1005/50V
C280
47pF/1005/50V
C281
1000pF/1005/25V
L34
1uH
IHLP2020CZER1R0M01
D29
B340A-E3/61T
C267
68pF/1005/50V
TP6
TP
2p5v
C219
22uF/2012/10V
C214
0.1uF/1005/6.3V
R209
0/1608
R208
21.5K/1608/1%
R211
10K/1608/1%
R210
0/1608
5v
100K/1608
R242
R212
33K/1005/1%
C215
220pF/1005/50V
C266
47pF/1005/50V
C216
1000pF/1005/25V
R245
68.1K/1005/1%
R197
14.3K/1005/1%
2p5v
3p3v_or_2p5v
3p3v
POW_SEL
J13
R189
0/6432/1W(N.M)
T3B-SQ(LF)(SN)
共振解析結果追加
3p3v_or_2p5v
C327
0.1uF/1005/6.3V
C328
0.1uF/1005/6.3V
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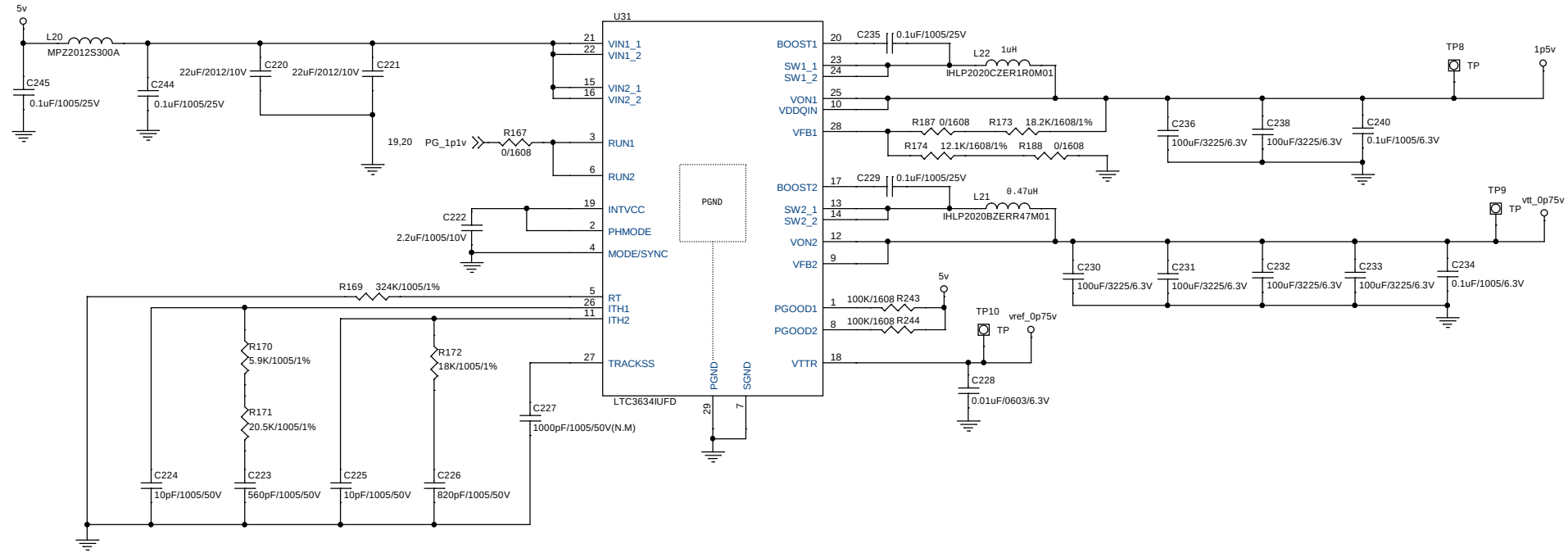

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