Reference Manual

Mpression Borax Card

Revision 1.0

2014/07/11

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1. For Ensuring Safe Use

Be sure to follow the instructions given in this Manual which are intended to prevent harm to the user and others as well as material damage.

1.1 Legend

Danger	Indicates an imminent hazardous situation which if not avoided will result in death or serious injury.
Warning	Indicates a potentially hazardous situation which if not avoided could result in death or serious injury.
Caution	Indicates a potentially hazardous situation which if not avoided may result in minor or moderate injury or in property damage.

1.2 Cautions

Danger	Make sure to use the AC adapter (included in package) that is specified in this Manual. Using an AC adapter not meeting the specifications described in this Manual will cause the kit to emit heat, explode, or ignite.
Warning	Do not apply strong impacts or blows to the kit. Doing so may cause the kit to emit heat, explode, or ignite, or the equipment in the kit to fail or malfunction. This may also cause fire.
	Do not put the main unit or the AC adapter in cooking appliances such as microwave ovens, or high-pressure containers. Doing so might cause the main unit or AC adapter to emit heat, explode, ignite, or emit smoke, or its parts to break or warp.
	Do not wrap the main unit that is in use with cloth or other materials that are likely to allow heat to build up inside the wrapping. This will cause heat to build up inside the wrapping which may cause the main unit to ignite or malfunction.
	When disposing of the main unit, do not dispose of it along with general household waste. Throwing the main unit into fire may cause it to explode. Dispose of the main unit following the laws, regulations, and ordinances governing waste disposal. Do not use the kit in places subject to extremely high or low temperatures or severe temperature changes. Doing so may cause the kit to fail or to malfunction. Always be sure to use the kit in a temperatures ranging from 5°C to 35°C and a humidity range of 0% to 85%.

Warning (Continued from previous page)	Do not pull the power supply cable with excessive force or place heavy items on it. Do not damage, break, bundle, or tamper with the power supply cable. Damaged parts of the power supply cable might cause a short circuit resulting in fire or accidents involving electrical shock.
	Do not unplug the power plug with wet or moist hands. This might cause injuries or equipment malfunctions or failures due to electrical shock.
	Plug the power plug securely into the outlet. If the power plug is not securely plugged into the outlet, it may cause accidents involving electrical shock or fire due to heat emitted.
	Do not connect many electrical cords to a single socket or connect an AC adapter to an outlet that is not rated for the specified voltage. Failing to do so may cause the equipment to malfunction or fail, or lead to accidents involving electrical shock or fire due to heat emitted.
	Periodically remove any dust accumulated on the power plug and around the outlet (socket). Do not use a power plug with dust accumulated on it because doing so will lead to insulation failure due to moisture which may lead to fire. Remove any dust on the power plug and around the outlet with dried cloth.
	Do not place any containers such as cups or vases filled with water or other liquid on this Board. If this Board is exposed to water or other liquids it may cause the Board to malfunction or lead to accidents involving electrical shock. If you spilled water or other liquid on this Board, immediately stop using the Board, turn off the power, and unplug the power plug. If you have any requests for repairs or technical consultation, please contact the Manufacturer.
Caution	Do not place the kit on unstable places such as shaky stands or tilted locations. Doing so may cause injuries or cause this Board to malfunction if the Board should fall.
	Do not attempt to use or leave the kit in places subject to strong direct sunlight or other places subject to high temperatures such as in cars in hot weather. Doing so might cause the kit to emit heat, break, ignite, run out of control, warp, or malfunction. Also, some parts of the equipment might emit heat causing burn injuries.
	Unplug the power supply cable when carrying out maintenance of devices in which the main unit is embedded. Failure to do so may lead to accidents involving electrical shock.
	Do not place this Board in locations where excessive force is applied to the Board. Failure to do so may cause the PC board to warp, leading to breakage of the PC board, missing parts or malfunctioning parts.
	When using the kit together with expansion boards or other peripheral devices, be sure to carefully read each of their manuals and to use them correctly. Manufacturer does not guarantee the operation of specific expansion boards or peripheral devices when used in conjunction with this Board unless they are specifically mentioned in this Manual or their successful operation with this Board has been confirmed in separate documents.

Caution (Continued from previous page)	Be sure to turn off the power switch when moving this Board to connect to other devices. Failure to do so may cause this Board to fail or lead to accidents involving electrical shock.
	Do not clean this Board by using a rag containing chemicals such as benzine or thinner. Failure to do so will likely to cause this Board to deteriorate. When using a chemical cloth be sure to comply with any directions or warnings.
	Do not immediately turn on the power if you find that water or moisture had condensed onto the main unit after removing the board from the package. Condensation might occur on this Board when taking it out of the box, if the board is cool yet the room temperature is warm. Do not apply power to the Board while water or moisture has condensed on it because the moisture may cause the Board to break or may shorten the service life of the parts. When you first take this Board out of the box be sure to leave it at room temperature for a while before using it. If condensation or moisture has occurred on this Board, first wait for the moisture to fully evaporate before installing or connecting the Board to other devices.
	Do not disassemble, dismantle, modify, alter, or recycle parts unless they are clearly described as customizable in this Manual. Although this kit is customizable, if parts not specified in this Manual as customizable are modified in any way, then the overall product operation cannot be guaranteed. Please consult with Manufacturer beforehand if you wish to customize or modify any parts that are not described in this Manual as customizable.

1.3 Developer Information

The Developer of this product is:
Cytech Technology LTD.
Blues Dong, John Li, CHINA
http://www.cytech.com

1.4 Inquiries

In case you have any inquiries about the use this product, please contact your local Macnica company or make inquiries through the contact form in the following web site:
http://www.m-pression.com/contact

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2. Borax Card

2.1 Overview

Borax is an Altera SOC module card, will help us easily to use SOC chip in system design. Consider it as a minimal MCU system, only need expand peripherals what you need on the base board.

2.2 Borax card components

A. CPU, ARM Cortex-A9 dual/solo, It can be selected as dual core or single core chip；
B. FPGA, CycloneV series, support density from 25K LE to 110K LE；
C. Nand Flash, up to 4GB；
D. QSPI Flash, up to 128MB；
E. DDR3 memory, up to 1GB；
F. One 10/100/1000M Ethernet MAC, RGMII interface with ETH PHY；
G. One USB OTG PHY；
H. One RTC, I2C interface with HPS；
I. HPS user I/O expand, has 8 input/output pins and 14 input only pins;
J. FPGA user I/O expand, has 123 input/output (including 6 RX LVDS) pins and 12 TX LVDS pins;
K. Temperature and voltages monitor on board.

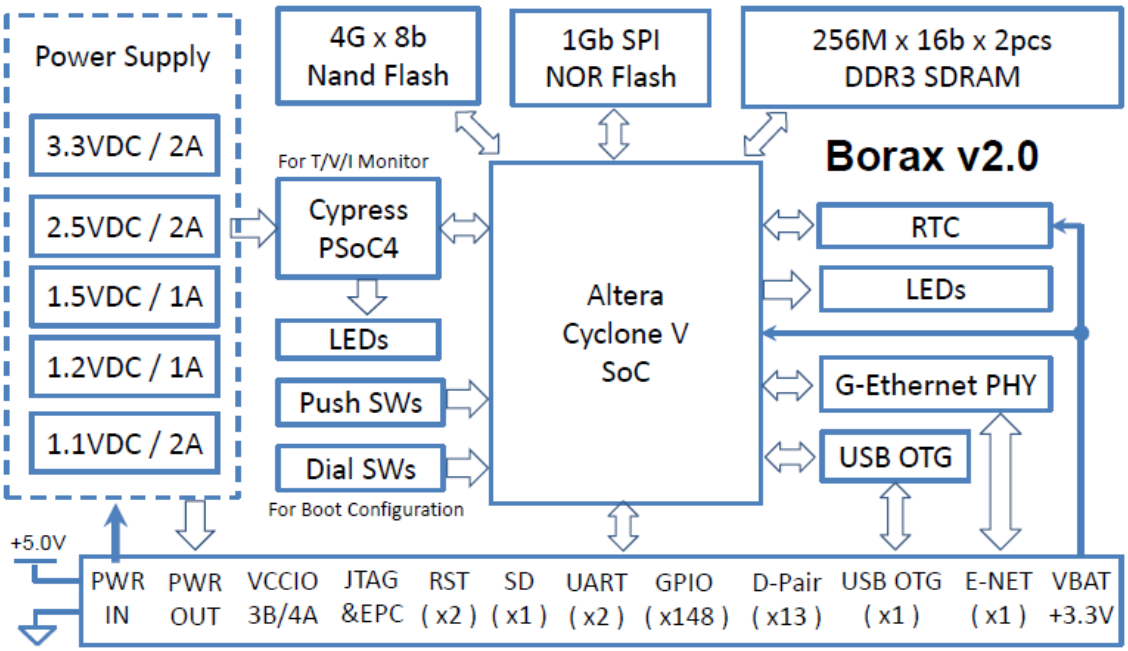

Figure 2-1 Borax block diagram

2.3 HPS Memory Features

2.3.1 QSPI Flash:

Borax Card boot from QSPI Flash as default. Preloader and UBOOT are saved in it.
Currently, Borax Card used 32MB QSPI Flash on board and the erase block is 64KB. The capacity is supported from 16MB to 128MB.
Because QSPI Flash is NOR flash that has much better reliability than NAND flash, so we used QSPI Flash as boot chip. Also, preloader and UBOOT saved in it for never erasing to preserve card from booting crash.

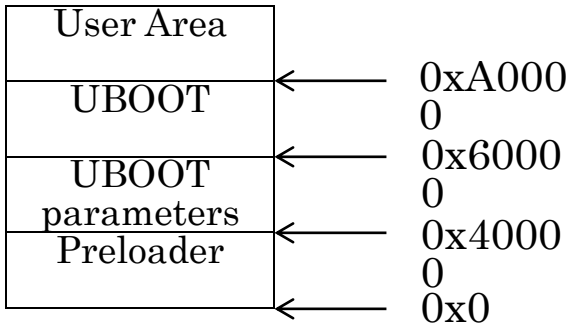

Figure 2-2 QSPI map

2.3.2 NAND Flash:

It is used to save Linux device tree file, kernel image, file system and FPGA configuration file. Default, Borax Card used 4GB NAND Flash on board and the erase block is 1MB, page size is 4KB.

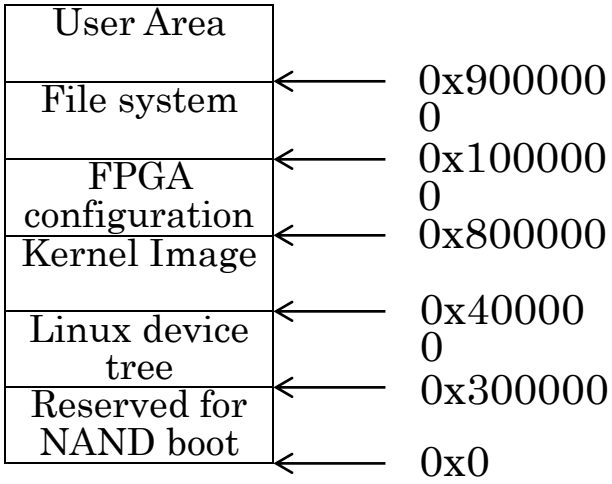

Figure 2-3 NAND map

2.3.3 DDR3

Two descrete DDR3 chips; 32 bit data width; 256MB~1GB capacity can be selected; Currently, we used 1GB on board. Support up to 800Mbps data bandwidth.

2.4 HPS Peripheral Features

2.4.1 Ethernet

Borax Card used HPS EMAC0 as primary Ethernet MAC peripheral, and put MICREL KSZ9031RNX PHY on board to connect with it. The output pins via connector to connect base board RJ45 for Ethernet connection.

U2 KSZ9031RNX	**J4** Connector
TX_A+	PIN 50
TX_A-	PIN 48
TX_B+	PIN 54
TX_B-	PIN 52
TX_C+	PIN 49
TX_C-	PIN 47
TX_D+	PIN 53
TX_D-	PIN 51

Table 2-1 Ethernet

2.4.2 USB OTG

Borax Card set HPS USB0 as USB OTG peripheral, and put USB3300 as PHY chip on the board.

U6 USB3300	J3 Connector
USB_VBUS	PIN 35
USB_DM	PIN 37
USB_DP	PIN 39
USB_ID	PIN 41

Table 2-2 USB OTG

2.4.3 RTC

Borax Card put RTC chip on board via I2C interface connecting with HPS. It is for Linux system date reserving. If you need keep the date after board power off, please connect the RTC power pin to your base board battery source pin.

U27 RTC	J3 Connector
RTC_BAT	PIN 3

Table 2-3 RTC battery

2.4.4 UART

Borax Card used HPS UART0 and UART1, those pins output to the connectors.
Default, we didn't use flow control function, so UART0_CTS, UART0_RTS, UART1_CTS, UART0_RTS can be used as HPS GPIO.

HPS UART	P1 FPGA	J4 Connector
UART0_TX	PIN_H17	PIN 1
UART0_RX	PIN_A17	PIN 2
UART0_CTS	PIN_A18	PIN 9
UART0_RTS	PIN_C17	PIN 11
UART1_TX	PIN_B16	PIN 3
UART1_RX	PIN_C19	PIN 4
UART1_CTS	PIN_B18	PIN 10
UART1_RTS	PIN_J17	PIN 12

Table 2-4 UART

2.5 HPS Reset, Clock, BSEL, CSEL

2.5.1 Reset

HPS has two types external reset pins, cold reset and warm reset.

HPS Reset	P1 FPGA	Connector
HPS_nRST (warm)	PIN_A23	J4 PIN_45
HPS_nPOR (cold)	PIN_H19	J3 PIN_5

Table 2-5 HPS Reset pins

2.5.2 Clock

On board 25MHz OSC for HPS CLK1 and CLK2.

2.5.3 BSEL

Default BSEL setting is 3'b111, set QSPI Flash as boot chip.

HPS BSEL	Pull up	Pull down
BSEL 0	R162 (default)	R112
BSEL 1	R163 (default)	R113
BSEL 2	R164 (default)	R131

Table 2-6 HPS MSEL

2.5.4 CSEL

Default CSEL setting is 2'b00.

HPS CSEL	Pull up	Pull down
CSEL 0	R166	R167 (default)
CSEL 1	R170	R172 (default)

Table 2-7 HPS CSEL

2.6 I/O Features

2.6.1 HPS I/O

There are two types HPS I/O. One is HPS input only pins, the other is HPS in/out pins.

For input only pins, they are located in Bank 6 with DDR3 interface, supporting 1.5V VCCIO.

HPS GPI	P1 FPGA	Connectors
HPS_6A6B_GPI0	PIN_M25	J4 PIN_59
HPS_6A6B_GPI1	PIN_K27	J6 PIN_1
HPS_6A6B_GPI2	PIN_R20	J4 PIN_39
HPS_6A6B_GPI3	PIN_R21	J4 PIN_41
HPS_6A6B_GPI4	PIN_R28	J6 PIN_5
HPS_6A6B_GPI5	PIN_P26	J6 PIN_3
HPS_6A6B_GPI6	PIN_T17	J4 PIN_34
HPS_6A6B_GPI7	PIN_T16	J4 PIN_29
HPS_6A6B_GPI8	PIN_Y28	J6 PIN_6
HPS_6A6B_GPI9	PIN_Y26	J6 PIN_4
HPS_6A6B_GPI10	PIN_U15	J4 PIN_27
HPS_6A6B_GPI11	PIN_U16	J4 PIN_31
HPS_6A6B_GPI12	PIN_AC27	J6 PIN_12
HPS_6A6B_GPI13	PIN_V24	J6 PIN_2

Table 2-8 HPS GPI

For in/out pins, they are located in Bank 7, supporting 3.3V VCCIO.

HPS GPI	P1 FPGA	Connectors
HPS_7A_IO0	PIN_C21	J4 PIN_63
HPS_7A_IO1	PIN_A22	J4 PIN_70
HPS_7A_IO2	PIN_B21	J4 PIN_67
HPS_7A_IO3	PIN_A21	J4 PIN_68
HPS_7A_IO4	PIN_K18	J4 PIN_61
HPS_7A_IO5	PIN_A20	J4 PIN_62
HPS_7A_IO6	PIN_J18	J4 PIN_57
HPS_7A_IO7	PIN_C16	J4 PIN_66

Table 2-9 HPS GPIO

2.6.2 FPGA I/O

We put Bank3A, 3B, 4A, 5A I/O to the connectors.

For Bank3A, VCCIO 3.3V

P1 FPGA	Connectors
PIN_Y8	J3 PIN_11
PIN_Y4	J3 PIN_17
PIN_W8	J3 PIN_13
PIN_Y5	J3 PIN_15
PIN_T8	J3 PIN_9
PIN_AB4	J3 PIN_19
PIN_U9	J3 PIN_7

Table 2-10 FPGA Bank3A GPIO

For Bank3B, VCCIO can be set as you need, default is 3.3V. Also, we reserved 3 pairs LVDS TX pins in this bank, if use them please set the bank VCCIO to 2.5V.

FPGA GPIO	P1 FPGA	Connectors
5CSX_3B_IO0	PIN_W11	J5 PIN_13
5CSX_3B_IO1	PIN_V11	J5 PIN_14
5CSX_3B_IO2	PIN_AF4	J5 PIN_25
5CSX_3B_IO3	PIN_AE9	J5 PIN_7
5CSX_3B_IO4	PIN_AE4	J5 PIN_21
5CSX_3B_IO5	PIN_AD10	J4 PIN_7
5CSX_3B_IO6	PIN_U11	J5 PIN_11
5CSX_3B_IO7	PIN_AF8	J3 PIN_67
5CSX_3B_IO8	PIN_T11	J5 PIN_12
5CSX_3B_IO9	PIN_AE7	J5 PIN_17
5CSX_3B_IO10	PIN_AF9	J3 PIN_68
5CSX_3B_IO11	PIN_AE11	J5 PIN_34
5CSX_3B_IO12	PIN_AE8	J5 PIN_15
5CSX_3B_IO13	PIN_AD11	J4 PIN_8
5CSX_3B_IO14	PIN_AF6	J5 PIN_27
5CSX_3B_IO15	PIN_AF5	J5 PIN_23
5CSX_3B_IO16	PIN_AG6	J5 PIN_29
5CSX_3B_IO17	PIN_AF10	J5 PIN_33
5CSX_3B_IO18	PIN_AF7	J3 PIN_70
5CSX_3B_IO19	PIN_AF11	J5 PIN_31
5CSX_3B_IO20	PIN_T12	J5 PIN_9
5CSX_3B_IO21	PIN_T13	J5 PIN_10
5CSX_3B_IO22	PIN_AD12	J5 PIN_30
5CSX_3B_IO23	PIN_AE12	J5 PIN_32

Table 2-11 FPGA Bank3B GPIO

FPGA GPIO	P1 FPGA	Connectors
5CSX_IOp9	PIN_AH6	J3 PIN_56
5CSX_IOn9	PIN_AH5	J3 PIN_58
5CSX_IOp10	PIN_AH3	J3 PIN_61
5CSX_Ion10	PIN_AH2	J3 PIN_63
5CSX_IOp11	PIN_AG5	J3 PIN_57
5CSX_Ion11	PIN_AH4	J3 PIN_59

Table 2-12 FPGA Bank3B LVDS TX

Borax card also reserved 5 pairs LVDS RX channels in Bank 3B that shared with GPIO pins.

LVDS RX	FPGA GPIO	Connectors
RX_IOp0	5CSX_3B_IO21	J5 PIN_10
RX _IOn0	5CSX_3B_IO20	J5 PIN_9
RX _IOp1	5CSX_3B_IO8	J5 PIN_12
RX _IOn1	5CSX_3B_IO6	J5 PIN_11
RX _IOp2	5CSX_3B_IO1	J5 PIN_14
RX _IOn2	5CSX_3B_IO0	J5 PIN_13
RX _IOp3	5CSX_3B_IO23	J5 PIN_32
RX _IOn3	5CSX_3B_IO22	J5 PIN_30
RX _IOp4	5CSX_3B_IO19	J5 PIN_31
RX _IOn4	5CSX_3B_IO17	J5 PIN_33

Table 2-13 FPGA Bank3B LVDS RX

For Bank4A, VCCIO can be set as you need, default is 3.3V. Also, we reserved 9 pairs LVDS TX pins in this bank, if use them please set the bank VCCIO to 2.5V.

FPGA GPIO	P1 FPGA	Connectors
5CSX_4A_IO0	PIN_AF13	J4 PIN_32
5CSX_4A_IO1	PIN_AG8	J3 PIN_65
5CSX_4A_IO2	PIN_AG13	J4 PIN_30
5CSX_4A_IO3	PIN_U13	J4 PIN_22
5CSX_4A_IO4	PIN_U14	J4 PIN_21
5CSX_4A_IO5	PIN_AE15	J4 PIN_37
5CSX_4A_IO6	PIN_AF15	J3 PIN_40
5CSX_4A_IO7	PIN_AG16	J3 PIN_38
5CSX_4A_IO8	PIN_AH12	J3 PIN_33
5CSX_4A_IO9	PIN_AF17	J3 PIN_22
5CSX_4A_IO10	PIN_V13	J4 PIN_20
5CSX_4A_IO11	PIN_W14	J4 PIN_18
5CSX_4A_IO12	PIN_AE17	J6 PIN_33
5CSX_4A_IO13	PIN_AD17	J4 PIN_40
5CSX_4A_IO14	PIN_AD19	J4 PIN_44
5CSX_4A_IO15	PIN_AF18	J3 PIN_43
5CSX_4A_IO16	PIN_AE19	J6 PIN_32
5CSX_4A_IO17	PIN_AA18	J6 PIN_7

5CSX_4A_IO18	PIN_AA19	**J6** PIN_11
5CSX_4A_IO19	PIN_AD20	**J4** PIN_46
5CSX_4A_IO20	PIN_AE20	**J3** PIN_45
5CSX_4A_IO21	PIN_AG20	**J3** PIN_28
5CSX_4A_IO22	PIN_AF20	**J3** PIN_30
5CSX_4A_IO23	PIN_AF21	**J3** PIN_31
5CSX_4A_IO24	PIN_AG21	**J3** PIN_27
5CSX_4A_IO25	PIN_AF22	**J3** PIN_25
5CSX_4A_IO26	PIN_AE22	**J6** PIN_30
5CSX_4A_IO27	PIN_AH21	**J3** PIN_26
5CSX_4A_IO28	PIN_AD23	**J6** PIN_25
5CSX_4A_IO29	PIN_AF23	**J3** PIN_12
5CSX_4A_IO30	PIN_AG23	**J3** PIN_23
5CSX_4A_IO31	PIN_AH24	**J3** PIN_21
5CSX_4A_IO32	PIN_AG24	**J3** PIN_10
5CSX_4A_IO33	PIN_AE23	**J3** PIN_24
5CSX_4A_IO34	PIN_AG26	**J6** PIN_31
5CSX_4A_IO35	PIN_AE24	**J6** PIN_27
5CSX_4A_IO36	PIN_AC23	**J6** PIN_23
5CSX_4A_IO37	PIN_AH26	**J3** PIN_6
5CSX_4A_IO38	PIN_AC22	**J6** PIN_21
5CSX_4A_IO39	PIN_AH27	**J3** PIN_4
5CSX_4A_IO40	PIN_AG25	**J3** PIN_8
5CSX_4A_IO41	PIN_AG28	**J6** PIN_26
5CSX_4A_IO42	PIN_AF25	**J6** PIN_29
5CSX_4A_IO43	PIN_AF28	**J6** PIN_22
5CSX_4A_IO44	PIN_AF27	**J6** PIN_24

Table 2-14 FPGA Bank4A GPIO

FPGA GPIO	**P1** FPGA	Connectors
5CSX_IOp0	PIN_AH23	**J3** PIN_14
5CSX_IOn0	PIN_AH22	**J3** PIN_16
5CSX_IOp1	PIN_AG19	**J3** PIN_18
5CSX_IOn1	PIN_AH19	**J3** PIN_20
5CSX_IOp2	PIN_AG18	**J3** PIN_46
5CSX_IOn2	PIN_AH18	**J3** PIN_44
5CSX_IOp3	PIN_AH17	**J3** PIN_48
5CSX_IOn3	PIN_AH16	**J3** PIN_50
5CSX_IOp4	PIN_AG15	**J3** PIN_52
5CSX_IOn4	PIN_AH14	**J3** PIN_54
5CSX_IOp5	PIN_AG14	**J3** PIN_53
5CSX_IOn5	PIN_AH13	**J3** PIN_55
5CSX_IOp6	PIN_AG11	**J3** PIN_36
5CSX_IOn6	PIN_AH11	**J3** PIN_34
5CSX_IOp7	PIN_AG10	**J3** PIN_60
5CSX_IOn7	PIN_AH9	**J3** PIN_62

5CSX_IOp8	PIN_AG9	**J3** PIN_64
5CSX_IOn8	PIN_AH8	**J3** PIN_66

Table 2-15 FPGA Bank4A LVDS TX

For Bank5A, VCCIO can be set as 3.3V or 2.5V, default is 3.3V.

FPGA GPIO	**P1** FPGA	Connectors
5CSX_5A_IO0	PIN_AA20	**J6** PIN_13
5CSX_5A_IO1	PIN_AE26	**J6** PIN_18
5CSX_5A_IO2	PIN_Y19	**J6** PIN_9
5CSX_5A_IO3	PIN_AE25	**J6** PIN_28
5CSX_5A_IO4	PIN_AD26	**J6** PIN_16
5CSX_5A_IO5	PIN_AC24	**J6** PIN_14
5CSX_5A_IO6	PIN_AB23	**J6** PIN_19
5CSX_5A_IO7	PIN_W15	**J3** PIN_51
5CSX_5A_IO8	PIN_Y17	**J4** PIN_24
5CSX_5A_IO9	PIN_Y18	**J4** PIN_42
5CSX_5A_IO10	PIN_Y16	**J3** PIN_49
5CSX_5A_IO11	PIN_AA24	**J6** PIN_17
5CSX_5A_IO12	PIN_V16	**J4** PIN_28
5CSX_5A_IO13	PIN_AA23	**J6** PIN_15
5CSX_5A_IO14	PIN_V15	**J4** PIN_25

Table 2-16 FPGA Bank5A GPIO

2.6.3 FPGA CLOCK

On board Clock 50MHz input for FPGA fabric located in Bank 5B PIN_Y24 that only 5CSE A5/A6 chip support. Other FPGA GCLK inputs locate to connectors, including one pair differential clock input located in Bank 4A.

FPGA Clock	**P1** FPGA	Connectors
5CSX_CLK0	PIN_W12 (Bank 3B)	**J5** PIN_22
5CSX_CLK1	PIN_V12 (Bank 3B)	**J4** PIN_17
5CSX_CLK2	PIN_AA13 (Bank 4A)	**J4** PIN_35
5CSX_CLK3	PIN_Y13 (Bank 4A)	**J5** PIN_24
5CSX_CLK4	PIN_D12 (Bank 8A)	**J5** PIN_2
5CSX_CLK5	PIN_C12 (Bank 8A)	**J4** PIN_23
5CSX_CLK6	PIN_W21 (Bank 5B)*	**J4** PIN_38
5CSX_CLK7	PIN_W20 (Bank 5B)*	**J4** PIN_36
5CSX_CLKp	PIN_Y15 (Bank 4A)	**J5** PIN_26
5CSX_CLKn	PIN_AA15 (Bank 4A)	**J5** PIN_28

Table 2-17 FPGA Clocks

***: Only 5CSE A5/A6 chip can use these clock input pins!**

2.6.4 VCCIO supporting

For I/O using flexibly, Borax has VCCIO options for your selection.

FPGA VCCIO	Default setting	Optional setting	External setting
Bank 3A	3.3V	--	--
Bank 3B	3.3V	2.5V	**J3** PIN_47
Bank 4A	3.3V	2.5V	**J3** PIN_29
Bank 5A	2.5V	3.3V	--
Bank 5B*	2.5V	--	--
Bank 6A/B	1.5V	--	--
Bank 7A/B/C	3.3V	--	--
Bank 7D	2.5V	--	--
Bank 8A	2.5V	--	--

Table 2-18 FPGA VCCIO

***: Only 5CSE A5/A6 chip can use Bank 5B pins!**

1. Set Bank 3B/4A VCCIO with 3.3V, put resistors R96, R31 and R98 on board;
2. Set Bank 3B/4A VCCIO with 2.5V, put resistors R160, R97 and R99 on board;
3. Set Bank 3B/4A VCCIO with external VCC supply, put resistors R30, R161 and R99 on board.

Please note that external VCCIO ≤ 2.5V.

2.6.5 VREF pins

All VREF pins are put to the connectors.

FPGA VCCIO	Connector
5CSX_VREF0	**J5** PIN_19
5CSX_VREF1	**J3** PIN_42
5CSX_VREF2	**J3** PIN_32
5CSX_VREF3	**J6** PIN_10
5CSX_VREF4	**J6** PIN_8
5CSX_VREF5	**J4** PIN_65
5CSX_VREF6	**J4** PIN_26

Table 2-19 FPGA VCCIO

2.7 FPGA Configuration

Borax supports three FPGA configuration modes, JTAG, FPP x16 and AS x1/x4.

2.7.1 JTAG

SOC has two JTAG chains for HPS and FPGA debugging and configuration. Borax make two JTAG chains connected serially, so using one JTAG port to touch two chains. JTAG pins send to connectors for external USB-Blaster connecting.

JTAG	Connector
JTAG_TCK	**J4** PIN_14
JTAG_TMS	**J4** PIN_69
JTAG_TDI	**J4** PIN_55
JTAG_TDO	**J4** PIN_15
JTAG_TRST	**J4** PIN_43

Table 2-20 JTAG pins

2.7.2 FPP

Default FPGA configuration mode is FPP x16 compression fast (MSEL=5'b00010). FPGA will be configured after HPS boot up in UBOOT environment. If you want change configuration mode, please modify MSEL selection mode on board.

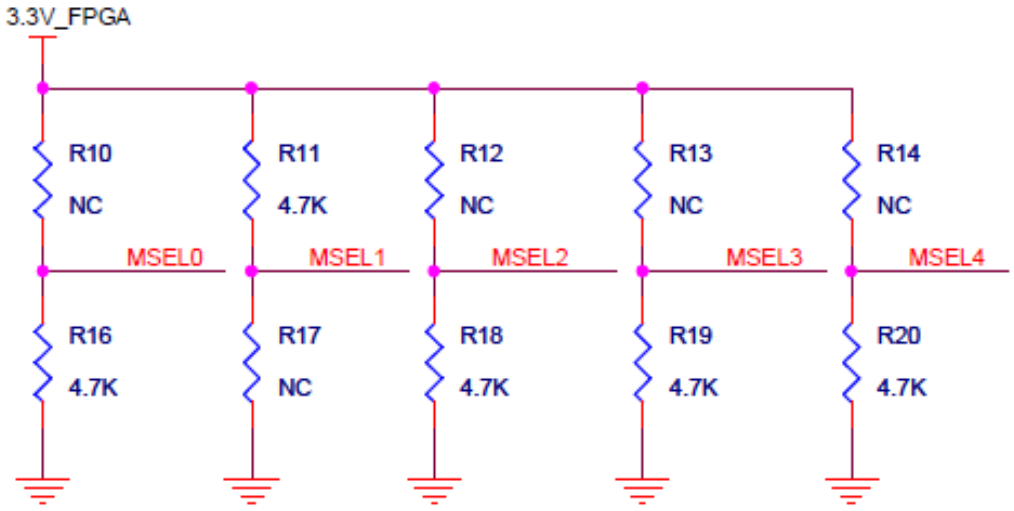

Figure 2-4 MSEL selection

2.7.3 AS

Borax put AS configuration pins to connectors for your convenience.

FPGA AS	Connector
EPCS_nCS	**J5** PIN_5
EPCS_DATA1	**J5** PIN_6
EPCS_DATA2	**J5** PIN_18
EPCS_DATA3	**J5** PIN_8
EPCS_ASDI	**J5** PIN_3
EPCS_DCLK	**J5** PIN_4

Table 2-21 FPGA AS configuration pins

3. Base Board

3.1 Borax Base board components

A. UART via USB interface;
B. USB OTG connector;
C. Ethernet RJ45 with Borax card ETH interface;
D. Ethernet PHY connected with FPGA I/O;
E. CAN interface with HPS;
F. SD card interface with FPGA I/O;
G. Touch LCD 800*480;
H. Six LED;
I. Four DIP switch;
J. Four push buttons;
K. On board USB2-Blaster II;

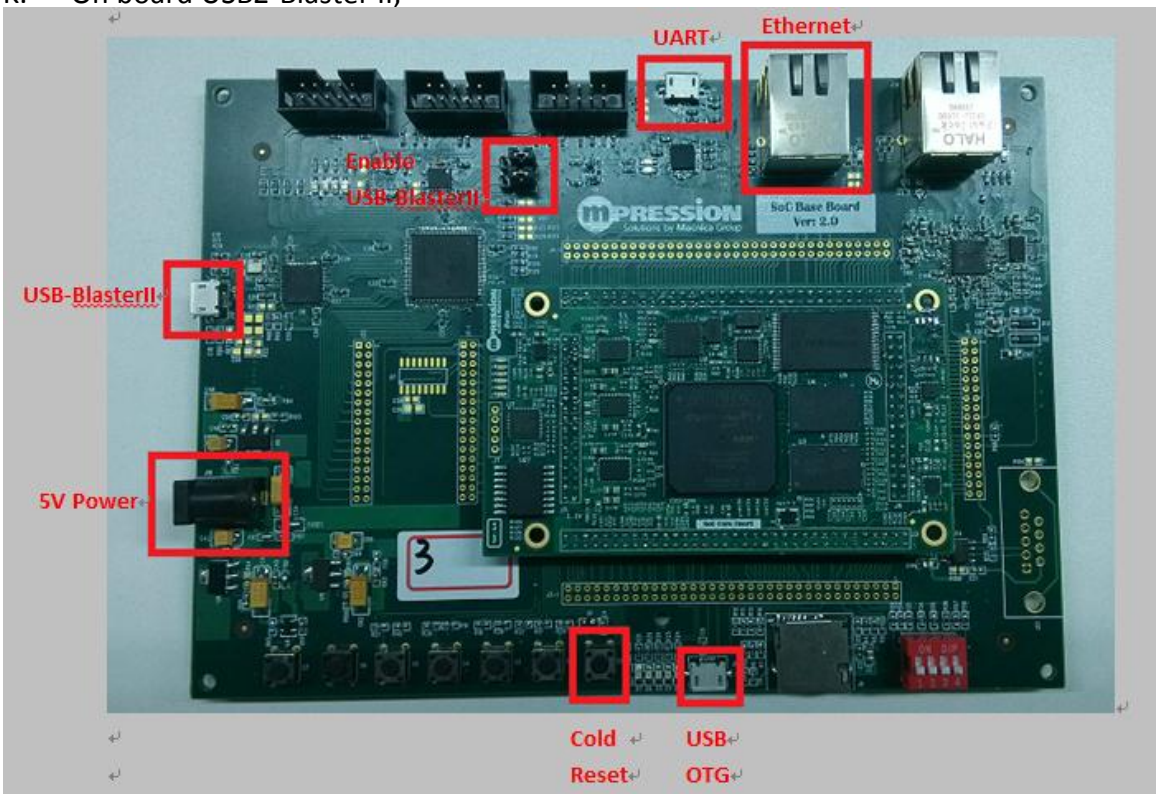

Figure 3-1 Borax base board

3.2 Assemble Borax Card

Please be sure that Borax Card connectors J3, J4 connect with base board J3, J4 connectors.

3.3 USB2-Blaster II

For JTAG chain connection, on board USB2-Blaster II or external USB-Blaster II can be selected. If using external USB-BlasterII, please connect to J15.

On board USB2-BlasterII	External USB-BlasterII
J18 1-2 on	J18 3-2 on
J19 1-2 on	J19 3-2 on

Table 3-1

3.4 UART

Base board uses a UART to USB converter for UART expanding. It connects with HPS UART0.

UART	J4 Connector
UART0_TX	PIN 1
UART0_RX	PIN 2

Table 3-2

3.5 USB

Base board has a direct connection with Borax USB OTG PHY.

USB OTG	J3 Connector
USB_VBUS	PIN 35
USB_DM	PIN 37
USB_DP	PIN 39
USB_ID	PIN 41

Table 3-3

3.6 Ethernet

Base board has two Ethernet ports. Port1 connect with HPS EMAC0 directly, because Borax card has PHY on board. Port2 is expanded from FPGA I/O with PHY on base board that using HPS EMAC1 through FPGA fabrics.

Port1	J4 Connector
TX_A+	PIN 50
TX_A-	PIN 48
TX_B+	PIN 54
TX_B-	PIN 52

TX_C+	PIN 49
TX_C-	PIN 47
TX_D+	PIN 53
TX_D-	PIN 51

Table 3-4 Port1

Port2	FPGA GPIO	Connectors
PHY_RXD0	5CSX_5A_IO1	**J6** PIN_18
PHY_RXD1	5CSX_5A_IO5	**J6** PIN_14
PHY_RXD2	5CSX_5A_IO4	**J6** PIN_16
PHY_RXD3	5CSX_4A_IO17	**J6** PIN_7
PHY_RX_CLK	5CSX_5A_IO6	**J6** PIN_19
PHY_RX_DV	5CSX_CLK1	**J4** PIN_17
PHY_TXD0	5CSX_5A_IO11	**J6** PIN_17
PHY_TXD1	5CSX_5A_IO13	**J6** PIN_15
PHY_TXD2	5CSX_5A_IO0	**J6** PIN_13
PHY_TXD3	5CSX_4A_IO18	**J6** PIN_11
PHY_GTX_CLK	5CSX_CLK2	**J4** PIN_35
PHY_TX_EN	5CSX_5A_IO2	**J6** PIN_9
PHY_MDC	5CSX_4A_IO38	**J6** PIN_21
PHY_MDIO	5CSX_4A_IO36	**J6** PIN_23
PHY_INTn	5CSX_4A_IO43	**J6** PIN_22
PHY_RESETn	5CSX_4A_IO44	**J6** PIN_24

Table 3-5 Port2

3.7 CAN

Base board CAN interface connect with HPS CAN.

CAN	HPS GPIO	**J4** Connector
CAN_TX	HPS_7A_IO6	PIN 57
CAN_RX	HPS_7A_IO5	PIN 62

Table 3-6

3.8 SD Card

Base board uses FPGA GPIO to expand SD card interface.

SD Card	FPGA	Connectors
SD_DAT0	PIN_Y8	**J3** PIN_11
SD_DAT1	PIN_Y4	**J3** PIN_17
SD_DAT2	PIN_W8	**J3** PIN_13
SD_DAT3	PIN_Y5	**J3** PIN_15

SD_CMD	PIN_T8	**J3** PIN_9
SD_CLK	PIN_AB4	**J3** PIN_19
SD_CD	PIN_U9	**J3** PIN_7

Table 3-7

3.9 LCD Touch Screen

Use FPGA GPIO to expand LCD drive interface.

LCD	FPGA GPIO	Connectors
LCD_VD0	5CSX_4A_IO29	**J3** PIN_12
LCD_VD1	5CSX_4A_IO12	**J6** PIN_33
LCD_VD2	5CSX_4A_IO34	**J6** PIN_31
LCD_VD3	5CSX_4A_IO16	**J6** PIN_32
LCD_VD4	5CSX_4A_IO42	**J6** PIN_29
LCD_VD5	5CSX_4A_IO26	**J6** PIN_30
LCD_VD6	5CSX_4A_IO35	**J6** PIN_27
LCD_VD7	5CSX_5A_IO3	**J6** PIN_28
LCD_VD8	5CSX_4A_IO28	**J6** PIN_25
LCD_VD9	5CSX_4A_IO41	**J6** PIN_26
LCD_VD10	5CSX_4A_IO9	**J3** PIN_22
LCD_VD11	5CSX_4A_IO31	**J3** PIN_21
LCD_VD12	5CSX_4A_IO33	**J3** PIN_24
LCD_VD13	5CSX_4A_IO30	**J3** PIN_23
LCD_VD14	5CSX_4A_IO27	**J3** PIN_26
LCD_VD15	5CSX_4A_IO25	**J3** PIN_25
LCD_VD16	5CSX_4A_IO21	**J3** PIN_28
LCD_VD17	5CSX_4A_IO24	**J3** PIN_27
LCD_VD18	5CSX_4A_IO22	**J3** PIN_30
LCD_VD19	5CSX_4A_IO23	**J3** PIN_31
LCD_VD20	5CSX_4A_IO7	**J3** PIN_38
LCD_VD21	5CSX_4A_IO6	**J3** PIN_40
LCD_VD22	5CSX_4A_IO15 *	**J3** PIN_43
LCD_VD23	5CSX_4A_IO20 *	**J3** PIN_45
LCD_VDEN	5CSX_5A_IO12	**J4** PIN_28
LCD_HSYNC	5CSX_4A_IO0	**J4** PIN_32
LCD_VSYNC	5CSX_4A_IO2	**J4** PIN_30
LCD_VCLK	5CSX_4A_IO5	**J4** PIN_37
LCD_PWR	5CSX_5A_IO10	**J3** PIN_49
LCD_PWM	5CSX_5A_IO8	**J4** PIN_24
LCD_nRESET	5CSX_5A_IO14	**J4** PIN_25

Table 3-8

***: Conflict with LED 0 and LED 1.**

3.10 LED, DIP Switch, Push Button

LED	FPGA GPIO	Connectors
LED 0	5CSX_4A_IO15 *	**J3** PIN_43
LED 1	5CSX_4A_IO20 *	**J3** PIN_45
LED 2	HPS_7A_IO1	**J4** PIN_70
LED 3	HPS_7A_IO2	**J4** PIN_67
LED 4	HPS_7A_IO3	**J4** PIN_68

Table 3-9

***: Conflict with LCD pins LCD_VD22 and LCD_VD23.**

DIP Switch	FPGA GPIO	Connectors
Dial_Switch0	5CSX_4A_IO32	**J3** PIN_10
Dial_Switch1	5CSX_4A_IO40	**J3** PIN_8
Dial_Switch2	5CSX_4A_IO37	**J3** PIN_6
Dial_Switch3	5CSX_4A_IO39	**J3** PIN_4

Table 3-10

Push Button	FPGA GPIO	Connectors
BUTTON 0	HPS_7A_IO0	**J4** PIN_63
BUTTON 1	HPS_7A_IO4	**J4** PIN_61
BUTTON 2	5CSX_3B_IO7	**J3** PIN_67
BUTTON 3	5CSX_3B_IO18	**J3** PIN_70

Table 3-11

4. Document Revision History

Date	Revision	Changes
July 11, 2014	1.0	• Document created
		•
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