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// This file is config test //single'//' indicates comment out. '//' is familiar
to verilog user.
#M : A                      //A:Altera
#S : 1                      //0:50M(def),1:25M,2:12.5M,3:8.333M,4:6.25M,5:5M
                            //6:3.125M,7:1.56M,8:0.78M,9:0.39M,F:Active
//Swap parameters
#P : SS = 1            //Swap bit
//#P : SB = 0          //Swap byte
//#P : SW = 0          //Swap word
//Preamble/Postamble parameters
#P : PR = 0000_0040    //Preamble insert Number by counting DCLK
#P : Po = 0000_8000    //Postamble insert Number by counting DCLK
//Delay parameters
#P : D0 = 0000_0100    //delay Number from nCONFIG to nSTATUS by counting 50MCLK
#P : D1 = 0000_0100    //delay Number from nSTATUS to DCLK by counting 50MCLK.
//Command parameters
#P : C0 = 1            //WordAligner
#P : C1 = 0            //nCONFIG,nSTATUS Pump ON
#P : C2 = 0            //MultiFPGA 2to1 x 4
#P : C3 = 0            //MultiFPGA 4to1 x 2
//#P : C9 = 1          //Version Information display on LED.
//Binary data area
//TEST_LED.RBF         //If binary file appear without "#n :",
                         //the binary file will select immediately.
#0 : TESTLED0.RBF      //rbf file
#1 : TESTLED1.POF      //pof file
#2 : TESTLED2.RBF      //rbf file
#3 : TESTLED3.POF      //pof file
#4 : TESTLED4.RBF
#5 : testled5.rbf
…
#F : TESTLEDF.rbf
//end
```