

MPE (Microchip Power Estimator)

V2021_R1.0
v2021.x

macnica

2022年3月

フィネッセカンパニー

技術統括部

消費電力計算ツール

● MPE (Microchip Power Estimator)

- スプレッド・シート・ベースの消費電力計算ツール
- 設計前でも電力見積もりが可能
- 動作周波数、デバイス型番、クロック、トグルレート、その他のパラメーターに基づいて電力モデルと組み合わせて、消費電力を推定

● 機能

- 迅速な電力見積もりのためにワークシートに統合されたシンプルなGUI
- アクティブモードとスタンバイモードでの電力見積もり
- シナリオを使用した電力見積もり
- デバイスの機能毎に電力見積もり可能な個別のワークシート
- ユーザー指定の温度入力に基づく T_j (接合部温度) の計算
- Libero SoC からのImport

消費電力見積もり

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入手方法

● Microchip メーカーページのURL

- <https://www.microsemi.com/product-directory/design-resources/1748-power-calculator>
- ファミリー毎のリンクより入手可能

Power Calculators

Overview

Use one of these family-specific excel-based power calculators to estimate power before using Libero SmartPower analysis.

RTG4 Power Estimator (UPDATED)	06/2021
RTG4 Power Estimator User Guide	6/2020
PolarFire and PolarFireSoC Power Estimator	04/2021
UG0897: PolarFire and PolarFire SoC FPGA Power Estimator User Guide	05/2021
SmartFusion2 and IGLOO2 Power Calculator	10/2019
SmartFusion2 and IGLOO2 Power Estimator User Guide	8/2014
SmartFusion Power Calculator	9/2011
IGLOO Power Calculator (applicable to IGLOO, IGLOOe, and IGLOO nano)	6/2011
ProASIC3 Power Calculator (applicable to ProASIC3, ProASIC3E, ProASIC3 nano, ProASIC3L, and RT ProASIC3)	6/2015
Fusion Power Calculator Estimator	1/2012
AX and RTAX-S/SLD Power Calculator	7/2013
eX, SX-A and RT54SX-S Power Calculator	2/2012
ProASIC ^{PLUS} Power Calculator	12/2004
ProASIC Power Calculator	3/2003

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Stay Informed

User Guide

- **詳細はUser Guide参照**

- PolarFire UG0897
- https://www.microsemi.com/document-portal/doc_download/1244575-ug0897-polarfire-and-polarfire-soc-fpga-power-estimator-user-guide
- SmartFusion2/IGLOO2 User Guide
- https://www.microsemi.com/document-portal/doc_download/132884-smartfusion2-and-igloo2-power-estimator-user-guide

MPEの起動

● DownloadしたExcelをオープン

Microchip Power Estimator (MPE) - v2021.2
PolarFire and PolarFire SoC

Powering FPGA

Settings

General

- Family: PolarFire
- Device: MP20K15L
- Package: FCB323
- Range: Extended
- Core Voltage: 1.0 V
- Process: Typical
- Speed Grade: STD
- Data Store: Protection

Power Summary

Category	Value
Total Power (W)	0.087
Low Power Mode (W)	0.007
Core Static (W)	0.000
IO (W)	0.000
Transceiver (W)	0.000
Junction Temperature Tj (°C)	25.00
Effective Theta JA (°C/W)	NA
Maximum Tj (°C)	NA
Thermal Margin	NA
Maximum Power (W)	NA

Modes and Scenarios

Mode	% Time in Mode	Power in Mode (W)	Power in scenario (W)
Active	100.00%	0.007	0.087
Static	0.00%	0.007	0.000

Power by Rails

Rail Name	Current (A)	Voltage (V)	Power (W)
VDD	0.245	1.200	0.294
VDDH1	0.000	1.800	0.000
VDDA15	0.000	3.300	0.000
VDDI 1.1	0.000	1.100	0.000
VDDI 1.2	0.000	1.200	0.000
VDDI 1.35	0.000	1.350	0.000
VDDI 1.5	0.000	1.500	0.000
VDDI 1.8	0.000	1.800	0.000
VDDI 2.5	0.000	2.500	0.000
VDDI 3.3	0.000	3.300	0.000
IOVH_VDD_0LX	0.000	3.300	0.000
VDDO5	0.000	2.500	0.011
VDDP	0.000	1.000	0.000
VDDPXA	0.000	2.500	0.000

Info

Type	Used	Total	Percentage (%)
SRF	0	192408	0%
SRAM	0	24	0%
ALUT	0	192408	0%
LSRAM	0	519	0%
uSRAM	0	1784	0%
Math Block	0	586	0%
PLL	0	3	0%
DLL	0	3	0%
ID	0	182	0%
Transceiver Labels	0	4	0%
Transceiver PCIe Hard Blocks	0	2	0%

使用方法 1

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使用方法1

● 設計前

- 詳細仕様が未定時での大まかな見積もり
- デバイス規模の使用率25/50/75/100% + 動作周波数で見積もり

デバイス選定

- “Settings”より選択

Microchip Power Estimator (MPE) - v2021.2
PolarFire and PolarFire SoC

Buttons: Import, Initialize Power Estimator, Manage IP, Create Snapshot, Reset to Defaults, Export Report

Project: [Empty]

Settings

General	
Family	PolarFire
Device	MPF300T
Package	FCG484
Range	Extended
Core Voltage	1.0 V
Process	Typical
Speed Grade	STD
Data State	Production

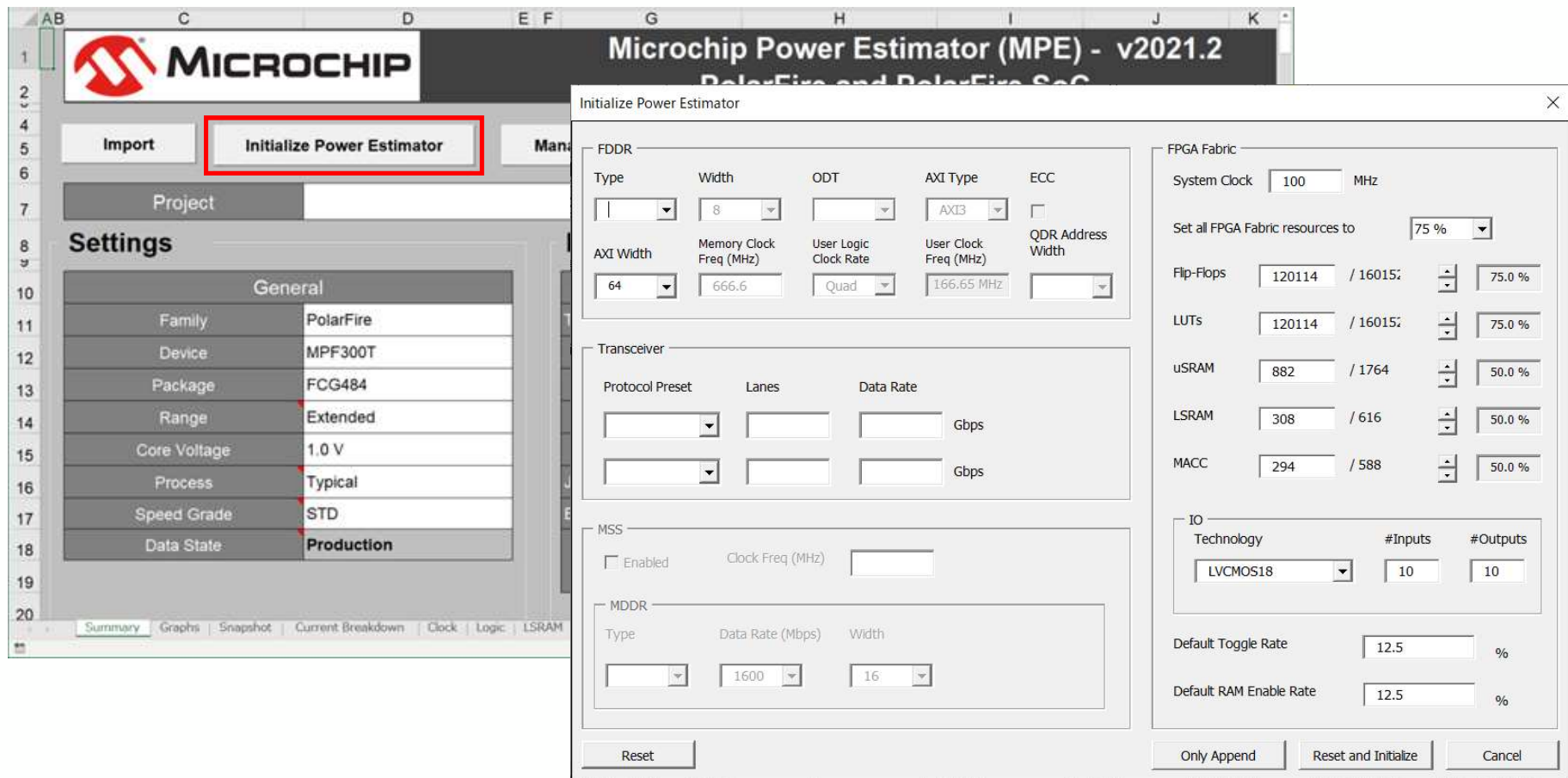
Power Summary

Summary		
Total Power (W)	0.917	
→ Device Static (W)	0.102	
→ Core Dynamic (W)	0.813	
→ I/O (W)	0.002	
→ Transceiver (W)	0.000	
Junction Temperature T _J (°C)	25.00	
Effective Theta JA (°C/W)	N/A	
Thermal Margin	Maximum Ta (°C)	N/A
	Maximum Power (W)	N/A

Bottom tabs: Summary, Graphs, Snapshot, Current Breakdown, Clock, Logic, LSRAM, uSRAM, Math Block, IO, Transceiver, PLL & DLL, User, Release

Initialize Power Estimatorをオープン

- “Initialize Power Estimator” ボタンを選択



使用率 + 動作周波数の設定

- “System Clock” MHzに動作周波数(Fmax)を入力
- “Set all FPGA Fabric Resources to”で25/50/75/100%を選択
- “Only Append”で決定、上書き確認で“はい”を選択

Initialize Power Estimator

FDDR

Type	Width	ODT	AXI Type	ECC
[]	8	[]	AXI3	<input type="checkbox"/>

AXI Width: 64 | Memory Clock Freq (MHz): 666.6 | User Logic Clock Rate: Quad | User Clock Freq (MHz): 166.65 MHz | QDR Address Width: []

Transceiver

Protocol Preset	Lanes	Data Rate
[]	[]	[] Gbps
[]	[]	[] Gbps

MSS

Enabled | Clock Freq (MHz): []

MDDR

Type	Data Rate (Mbps)	Width
[]	1600	16

FPGA Fabric

System Clock: 100 MHz

Set all FPGA Fabric resources to: 75 %

Resource	Current	Max	Usage
Flip-Flops	120114	160151	75.0 %
LUTs	120114	160151	75.0 %
uSRAM	882	1764	50.0 %
LSRAM	308	616	50.0 %
MACC	294	588	50.0 %

IO

Technology	#Inputs	#Outputs
LVC MOS18	10	10

Default Toggle Rate: 12.5 %
Default RAM Enable Rate: 12.5 %

Buttons: Reset, Only Append, Reset and Initialize, Cancel

Append and set to the values specified

This action will append data for all the user entry fields, except for device settings and set them to the values specified. Do you want to continue?

Buttons: はい, いいえ

結果の確認

- “Summary”で結果を確認

The screenshot displays the Microchip Power Estimator (MPE) v2021.2 interface for PolarFire and PolarFire SoC. The interface includes a top navigation bar with the Microchip logo and title, a toolbar with buttons for Import, Initialize Power Estimator, Manage IP, Create Snapshot, Reset to Defaults, and Export Report, and a Project field. The main area is divided into Settings and Power Summary sections.

Settings - General

Family	PolarFire
Device	MPF300T
Package	FCG484
Range	Extended
Core Voltage	1.0 V
Process	Typical
Speed Grade	STD
Data State	Production

Power Summary

Summary		
Total Power (W)		2.189
→ Device Static (W)		0.107
→ Core Dynamic (W)		2.079
→ I/O (W)		0.003
→ Transceiver (W)		0.000
Junction Temperature T _J (-C)		25.00
Effective Theta JA (-C/W)		N/A
Thermal Margin	Maximum Ta (-C)	N/A
	Maximum Power (W)	N/A

The "Summary" tab in the bottom navigation bar is highlighted with a red box.

使用方法2

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使用方法 2

- 仕様確定または設計中

- 詳細仕様が確定後または設計中で大まかな規模が設定可能

デバイス選定

- “Settings”より選択

Microchip Power Estimator (MPE) - v2021.2
PolarFire and PolarFire SoC

Buttons: Import, Initialize Power Estimator, Manage IP, Create Snapshot, Reset to Defaults, Export Report

Project: [Empty]

Settings

General	
Family	PolarFire
Device	MPF300T
Package	FCG484
Range	Extended
Core Voltage	1.0 V
Process	Typical
Speed Grade	STD
Data State	Production

Power Summary

Summary		
Total Power (W)	0.917	
→ Device Static (W)	0.102	
→ Core Dynamic (W)	0.813	
→ I/O (W)	0.002	
→ Transceiver (W)	0.000	
Junction Temperature T _J (°C)	25.00	
Effective Theta JA (°C/W)	N/A	
Thermal Margin	Maximum T _a (°C)	N/A
	Maximum Power (W)	N/A

Bottom tabs: Summary, Graphs, Snapshot, Current Breakdown, Clock, Logic, LSRAM, uSRAM, Math Block, IO, Transceiver, PLL & DLL, User, Release

各種シートで詳細設定

- “Clock”、“Logic”、“LSRAM”、“uSRAM”、“Math Block”、“IO”、“Transceiver”、“PLL & DLL” シートで詳細設定

Microchip Power Estimator (MPE) - v2021.2
PolarFire and PolarFire SoC

Buttons: Import, Initialize Power Estimator, Manage IP, Create Snapshot, Reset to Defaults, Export Report

Project: [Empty]

Settings

General	
Family	PolarFire
Device	MPF300T
Package	FCG484
Range	Extended
Core Voltage	1.0 V
Process	Typical
Speed Grade	STD
Data State	Production

Power Summary

Summary		
Total Power (W)	0.917	
→ Device Static (W)	0.102	
→ Core Dynamic (W)	0.813	
→ I/O (W)	0.002	
→ Transceiver (W)	0.000	
Junction Temperature Tj (-C)	25.00	
Effective Theta JA (-C/W)	N/A	
Thermal Margin	Maximum Ta (-C)	N/A
	Maximum Power (W)	N/A

Navigation tabs: Summary | Graphs | Snapshot | Current Breakdown | **Clock | Logic | LSRAM | uSRAM | Math Block | IO | Transceiver | PLL & DLL** | User | Release

Clockの設定

● “Clock”シートで入力

- 。クロック系統や周波数別に個別の名称で、周波数/Fanout 数を設定

The screenshot displays the 'Clock Tree Power' report. At the top, there is a 'Return to Summary' button. Below it, a table shows the power for the VDD rail: Voltage (V) is 1.000 and Power (W) is 0.410, which is 24% of the total power of 1.697 W. To the right, an 'Utilization' table shows: Global (3, 13%), Regional (ICLK) (0, 0%), Regional (LCLK) (0, 0%), and Bank Clock (0, 0%). There are links for 'Clocking Resources User Guide' and 'MPE User Guide'. The main table lists clock configurations with columns: Name, Clock Frequency (MHz), Clock Type, Fanout, Clock Buffer Enable Rate, and Power (W). The first three rows (SYS_CLK, RX_CLK, TX_CLK) are highlighted with a red border. The bottom navigation bar shows 'Clock' selected, with other tabs like Logic, LSRAM, uSRAM, Math Block, IO, Transceiver, PLL & DLL, User, and Release. The bottom right corner shows '表示設定' and a zoom level of 100%.

Name	Clock Frequency (MHz)	Clock Type	Fanout	Clock Buffer Enable Rate	Power (W)
SYS_CLK	100.00	Global	40000	100.0%	0.075
RX_CLK	148.50	Global	54000	100.0%	0.150
TX_CLK	125.00	Global	80000	100.0%	0.186
		Global		100.0%	0.000
		Global		100.0%	0.000
		Global		100.0%	0.000
		Global		100.0%	0.000

Logicの設定

● “Logic”シートで入力

- クロックシステムやコンポーネント名を個別の名称で、周波数/DFF数/4LUT数を設定

Name	Clock Frequency (MHz)	Number of DFF	Number of 4LUT	Design Complexity	Toggle Rate	Power (W)
SYS_CLK	100.00	40000	35000	3.0	12.5%	0.135
RX_CLK	148.50	54000	50000	3.0	12.5%	0.277
TX_CLK	125.00	80000	75000	3.0	12.5%	0.347
				3.0	12.5%	0.000
				3.0	12.5%	0.000
				3.0	12.5%	0.000
				3.0	12.5%	0.000
				3.0	12.5%	0.000
				3.0	12.5%	0.000
				3.0	12.5%	0.000

LSRAMの設定

● “LSRAM”シートで入力

- クロックシステムやコンポーネント名を個別の名称で、LSRAM Block数/Width(データ幅)/周波数などを設定

The screenshot displays the "LSRAM Power" spreadsheet. At the top, there are summary statistics for the VDD rail, showing a voltage of 1.000V and a power consumption of 0.119W, which is 7% of the total power of 1.706W. The utilization for LSRAM is shown as 708 blocks, representing 74% of the total. Below this, there are two sections for Port A and Port B, each with a table of LSRAM blocks. The table columns include Name, Number of LSRAM Blocks, Width, Clock Frequency (MHz), Write Mode, Write Rate, Read Rate, Enable Rate, and Power (W). The first three rows of the table (SYS_CLK, RX_CLK, TX_CLK) are highlighted with a red border, indicating they are the primary focus of the configuration. The bottom of the spreadsheet shows a navigation bar with tabs for Clock, Logic, LSRAM, uSRAM, Math Block, IO, Transceiver, PLL & DLL, User, and Release. The LSRAM tab is currently selected.

Rail		Voltage (V)	Power (W)	Utilization	
VDD	1.000	0.119	LSRAM	708	74%
7% of total power 1.706 W					

Port A										Port B							
Name	Number of LSRAM Blocks	Width	Clock Frequency (MHz)	Write Mode	Write Rate	Read Rate	Enable Rate	Width	Clock Frequency (MHz)	Write Mode	Write Rate	Read Rate	Enable Rate	Pipeline Enable	ECC Enable	Output Toggle Rate	Power (W)
SYS_CLK	308	20	100.00	Simple Write	12.5%	12.5%	12.5%	20	100.00	Simple Write	12.5%	12.5%	12.5%	No	No	50.0%	0.043
RX_CLK	200	20	148.50	Simple Write	12.5%	12.5%	12.5%	20	148.50	Simple Write	12.5%	12.5%	12.5%	No	No	50.0%	0.041
TX_CLK	200	20	125.00	Simple Write	12.5%	12.5%	12.5%	20	125.00	Simple Write	12.5%	12.5%	12.5%	No	No	50.0%	0.035
		20		Simple Write	12.5%	12.5%	12.5%	20		Simple Write	12.5%	12.5%	12.5%	No	No	50.0%	0.000
		20		Simple Write	12.5%	12.5%	12.5%	20		Simple Write	12.5%	12.5%	12.5%	No	No	50.0%	0.000
		20		Simple Write	12.5%	12.5%	12.5%	20		Simple Write	12.5%	12.5%	12.5%	No	No	50.0%	0.000
		20		Simple Write	12.5%	12.5%	12.5%	20		Simple Write	12.5%	12.5%	12.5%	No	No	50.0%	0.000
		20		Simple Write	12.5%	12.5%	12.5%	20		Simple Write	12.5%	12.5%	12.5%	No	No	50.0%	0.000
		20		Simple Write	12.5%	12.5%	12.5%	20		Simple Write	12.5%	12.5%	12.5%	No	No	50.0%	0.000
		20		Simple Write	12.5%	12.5%	12.5%	20		Simple Write	12.5%	12.5%	12.5%	No	No	50.0%	0.000
		20		Simple Write	12.5%	12.5%	12.5%	20		Simple Write	12.5%	12.5%	12.5%	No	No	50.0%	0.000
		20		Simple Write	12.5%	12.5%	12.5%	20		Simple Write	12.5%	12.5%	12.5%	No	No	50.0%	0.000
		20		Simple Write	12.5%	12.5%	12.5%	20		Simple Write	12.5%	12.5%	12.5%	No	No	50.0%	0.000
		20		Simple Write	12.5%	12.5%	12.5%	20		Simple Write	12.5%	12.5%	12.5%	No	No	50.0%	0.000
		20		Simple Write	12.5%	12.5%	12.5%	20		Simple Write	12.5%	12.5%	12.5%	No	No	50.0%	0.000
		20		Simple Write	12.5%	12.5%	12.5%	20		Simple Write	12.5%	12.5%	12.5%	No	No	50.0%	0.000
		20		Simple Write	12.5%	12.5%	12.5%	20		Simple Write	12.5%	12.5%	12.5%	No	No	50.0%	0.000
		20		Simple Write	12.5%	12.5%	12.5%	20		Simple Write	12.5%	12.5%	12.5%	No	No	50.0%	0.000

uSRAMの設定

● “uSRAM”シートで入力

- クロックシステムやコンポーネント名を個別の名称で、uSRAM Block数/Width(データ幅)/周波数などを設定

uSRAM Power											
Rail			Voltage (V)		Power (W)		Utilization			Fabric User Guide	
VDD	1.000	0.017	uSRAM	882	32%					MPE User Guide	
1% of total power 1.679 W											
Name	Number of uSRAM Blocks	Width	Use Registers	Write Clock Frequency (MHz)	Enable Rate	Read Port Clock Domain Frequency (MHz)	Enable Rate	Output Toggle Rate	Power (W)		
SYS_CLK	882	12	No	100.00	12.5%	100.00	12.5%	50.0%	0.017		
		12	No		12.5%		12.5%	50.0%	0.000		
		12	No		12.5%		12.5%	50.0%	0.000		
		12	No		12.5%		12.5%	50.0%	0.000		

Math Blockの設定

● “Math Block”シートで入力

- クロックシステムやコンポーネント名を個別の名称で、周波数/Math Block数 /Mode(ダウンリストより選択)などを設定

The screenshot shows a spreadsheet interface for configuring Math Block power. At the top, there is a 'Return to Summary' button and the title 'Math Block Power'. Below this, there are summary statistics for the rail voltage and power, and the utilization of Math Blocks. A table below lists individual Math Block configurations with columns for Name, Clock Frequency, Number of Math Blocks, Output Toggle Rate, Mode, Pre Adder, Pipelined Inputs, Pipelined Outputs, and Power (W). The first row of the table is highlighted with a red border.

Name	Clock Frequency (MHz)	Number of Math Blocks	Output Toggle Rate	Mode	Pre Adder	Pipelined Inputs	Pipelined Outputs	Power (W)
SYS_CLK	100.00	300	12.5%	Normal-Multiplier	No	No	No	0.104
			12.5%	Normal-Multiplier	No	No	No	0.000
			12.5%	Normal-Multiplier	No	No	No	0.000
			12.5%	Normal-Multiplier	No	No	No	0.000
			12.5%	Normal-Multiplier	No	No	No	0.000
			12.5%	Normal-Multiplier	No	No	No	0.000

IOの設定

● “IO”シートで入力

- クロック系統やIO Standardを個別の名称で、Bank Type/IO Standard/Input Pins/Output Pinsなどを設定

I/O Power

Rail	Voltage (V)	Current (A)	Power (W)
VDD	1.000	0.010	0.010
VDD18	1.800	0.000	0.001
VDDAUX	3.300	0.001	0.004
VDDI 1.1	1.100	0.000	0.000
VDDI 1.2	1.200	0.000	0.000
VDDI 1.35	1.350	0.000	0.000
VDDI 1.5	1.500	0.000	0.000
VDDI 1.8	1.800	0.002	0.004
VDDI 2.5	2.500	0.000	0.000
VDDI 3.3	3.300	0.001	0.003
XCVR_VDD_CLK	3.300	0.002	0.006
Total Power			0.028

2% of total power 1.544 W

MPF User Guide
I/O User Guide

Utilization	
Inputs	40 15%
Outputs	35 13%
Bidirectional	12 5%
HSIO	40 42%
GPIO	43 29%
XCVR_CLK	4 18%
I/O Count	87 33%

Name	Bank Type	IO Standard	Mixed Mode VDDI	Input Pins	Output Pins	Bidir Pins	VCM	Schmitt Trigger	ODT	Output Drive (mA) / Drive Impedance (Ohm)	Slew Calibration	Output Load (pF)	IOD Mode	I/O Activity				Thermal Power (W)				
														Clock (MHz)	Data Rate	Toggle Rate	Output Enable	VDD	VDD18	VDDAUX	VDDI	Total
ISYS_CLK	GPIO	LVTTL	3.3	10	10		Off	Off	NO_ODT	2 mA	Off	5 Unused		100.00	SDR	12.5%	50.0%	0.000	0.000	0.003	0.003	0.006
RX_CLK	GPIO	LVCNOS18	1.8	16	5	2	Off	Off	NO_ODT	8 mA	Off	5 RX_DDR_G_A 1		148.50	SDR	12.5%	50.0%	0.003	0.000	0.001	0.001	0.005
TX_CLK	HSIO	LVCNOS18	1.8	10	20	10	Off	Off	NO_ODT	8 mA	Off	5 TX_DDR_G 1		125.00	SDR	12.5%	50.0%	0.004	0.001	0.000	0.003	0.008
RX_REF_CLK	XCVR_REFCLK	HCSSL25	2.5	1			Off	Off	100	Off	Off	5 Unused		148.50	clock		50.0%	0.002	0.000	0.000	0.003	0.004
TX_REF_CLK	XCVR_REFCLK	HCSSL25	2.5	1			Off	Off	100	Off	Off	5 Unused		125.00	clock		50.0%	0.002	0.000	0.000	0.003	0.004
	HSIO	LVCNOS18	1.8				Off	Off	NO_ODT	2 mA	Off	5 Unused			SDR	12.5%	50.0%	0.000	0.000	0.000	0.000	0.000
	HSIO	LVCNOS18	1.8				Off	Off	NO_ODT	2 mA	Off	5 Unused			SDR	12.5%	50.0%	0.000	0.000	0.000	0.000	0.000
	HSIO	LVCNOS18	1.8				Off	Off	NO_ODT	2 mA	Off	5 Unused			SDR	12.5%	50.0%	0.000	0.000	0.000	0.000	0.000
	HSIO	LVCNOS18	1.8				Off	Off	NO_ODT	2 mA	Off	5 Unused			SDR	12.5%	50.0%	0.000	0.000	0.000	0.000	0.000
	HSIO	LVCNOS18	1.8				Off	Off	NO_ODT	2 mA	Off	5 Unused			SDR	12.5%	50.0%	0.000	0.000	0.000	0.000	0.000

IO Transceiver PLL & DLL User Release

Transceiverの設定

● “Transceiver”シートで入力

- クロック系統やコンポーネント名を個別の名称で、Lanes/Operational Mode/TX Data Rate(Gpbs)/RX Data Rate(Gbps)Width(データ幅)/PLL Used/Widthなどを設定

Return to Summary **Transceiver Power**

Rail	Voltage (V)	Current (A)	Power (W)
VDD	1.000	0.038	0.038
VDDA	1.000	0.172	0.038
VDDA25	2.500	0.047	0.117
Total Power			0.326
17% of total power 1.871 W			

Power (W) by Hard Block	
PMA	0.250
PCS	0.038
PCIe	0.000
Tx PLL	0.039

Utilization	
Lanes	8 100%
PCIe Blocks	0 0%

[Transceiver User Guide](#)
[MPC User Guide](#)

Name	Protocol Preset	Number of Lanes	Operational Mode	TX Data Rate (Gbps)	RX Data Rate (Gbps)	PMA			TX		PCS		Power				
						PLL Used	DFE Enable	Eye Monitor Enable	CTLE Drive	Amplitude (mV)	Mode	Width	Hard PCIe	VDD Power (W)	VDDA Power (W)	VDDA25 Power (W)	Total Power (W)
CXP+SLVS-EC		4	Independent Tx/Rx	12.5	5	Q0 TXPLL0	No	No	No Peak +2.8dB	400mV with -3.5dB	8b/10b	64	No	0.013	0.136	0.096	0.245
SLVS-EC		4	Rx Only		5	Q0 TXPLL0	No	No	No Peak +2.8dB	800mV with -6.0dB	8b/10b	32	No	0.025	0.036	0.021	0.082
	Duplex					Q0 TXPLL0	No	No	3GHz +1.4dB	200mV with 0dB	8b/10b	32	No	0.000	0.000	0.000	0.000
	Duplex					Q0 TXPLL0	No	No	3GHz +1.4dB	200mV with 0dB	8b/10b	32	No	0.000	0.000	0.000	0.000
	Duplex					Q0 TXPLL0	No	No	3GHz +1.4dB	200mV with 0dB	8b/10b	32	No	0.000	0.000	0.000	0.000
	Duplex					Q0 TXPLL0	No	No	3GHz +1.4dB	200mV with 0dB	8b/10b	32	No	0.000	0.000	0.000	0.000
	Duplex					Q0 TXPLL0	No	No	3GHz +1.4dB	200mV with 0dB	8b/10b	32	No	0.000	0.000	0.000	0.000
	Duplex					Q0 TXPLL0	No	No	3GHz +1.4dB	200mV with 0dB	8b/10b	32	No	0.000	0.000	0.000	0.000
	Duplex					Q0 TXPLL0	No	No	3GHz +1.4dB	200mV with 0dB	8b/10b	32	No	0.000	0.000	0.000	0.000
	Duplex					Q0 TXPLL0	No	No	3GHz +1.4dB	200mV with 0dB	8b/10b	32	No	0.000	0.000	0.000	0.000
	Duplex					Q0 TXPLL0	No	No	3GHz +1.4dB	200mV with 0dB	8b/10b	32	No	0.000	0.000	0.000	0.000
	Duplex					Q0 TXPLL0	No	No	3GHz +1.4dB	200mV with 0dB	8b/10b	32	No	0.000	0.000	0.000	0.000
	Duplex					Q0 TXPLL0	No	No	3GHz +1.4dB	200mV with 0dB	8b/10b	32	No	0.000	0.000	0.000	0.000
	Duplex					Q0 TXPLL0	No	No	3GHz +1.4dB	200mV with 0dB	8b/10b	32	No	0.000	0.000	0.000	0.000
	Duplex					Q0 TXPLL0	No	No	3GHz +1.4dB	200mV with 0dB	8b/10b	32	No	0.000	0.000	0.000	0.000
	Duplex					Q0 TXPLL0	No	No	3GHz +1.4dB	200mV with 0dB	8b/10b	32	No	0.000	0.000	0.000	0.000
	Duplex					Q0 TXPLL0	No	No	3GHz +1.4dB	200mV with 0dB	8b/10b	32	No	0.000	0.000	0.000	0.000
	Duplex					Q0 TXPLL0	No	No	3GHz +1.4dB	200mV with 0dB	8b/10b	32	No	0.000	0.000	0.000	0.000
	Duplex					Q0 TXPLL0	No	No	3GHz +1.4dB	200mV with 0dB	8b/10b	32	No	0.000	0.000	0.000	0.000
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	Duplex					Q0 TXPLL0	No	No	3GHz +1.4dB	200mV with 0dB	8b/10b	32	No	0.000	0.000	0.000	0.000
	Duplex					Q0 TXPLL0	No	No	3GHz +1.4dB	200mV with 0dB	8b/10b	32	No	0.000	0.000	0.000	0.000
	Duplex					Q0 TXPLL0	No	No	3GHz +1.4dB	200mV with 0dB	8b/10b	32	No	0.000	0.000	0.000	0.000
	Duplex					Q0 TXPLL0	No	No	3GHz +1.4dB	200mV with 0dB	8b/10b	32	No	0.000	0.000	0.000	0.000
	Duplex					Q0 TXPLL0	No	No	3GHz +1.4dB	200mV with 0dB	8b/10b	32	No	0.000	0.000	0.000	0.000
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	Duplex					Q0 TXPLL0	No	No	3GHz +1.4dB	200mV with 0dB	8b/10b	32	No	0.000	0.000	0.000	0.000
	Duplex					Q0 TXPLL0	No	No	3GHz +1.4dB	200mV with 0dB	8b/10b	32	No	0.000	0.000	0.000	0.000
	Duplex					Q0 TXPLL0	No	No	3GHz +1.4dB	200mV with 0dB	8b/10b	32	No	0.000	0.000	0.000	0.000
	Duplex					Q0 TXPLL0	No	No	3GHz +1.4dB	200mV with 0dB	8b/10b	32	No	0.000	0.000	0.000	0.000
	Duplex					Q0 TXPLL0	No	No	3GHz +1.4dB	200mV with 0dB	8b/10b	32	No	0.000	0.000	0.000	0.000
	Duplex					Q0 TXPLL0	No	No	3GHz +1.4dB	200mV with 0dB	8b/10b	32	No	0.000	0.000	0.000	0.000
	Duplex					Q0 TXPLL0	No	No	3GHz +1.4dB	200mV with 0dB	8b/10b	32	No	0.000	0.000	0.000	0.000
	Duplex					Q0 TXPLL0	No	No	3GHz +1.4dB	200mV with 0dB	8b/10b	32	No	0.000	0.000	0.000	0.000
	Duplex					Q0 TXPLL0	No	No	3GHz +1.4dB	200mV with 0dB	8b/10b	32	No	0.000	0.000	0.000	0.000
	Duplex					Q0 TXPLL0	No	No	3GHz +1.4dB	200mV with 0dB	8b/10b	32	No	0.000	0.000	0.000	0.000
	Duplex					Q0 TXPLL0	No	No	3GHz +1.4dB	200mV with 0dB	8b/10b	32	No	0.000	0.000	0.000	0.000
	Duplex					Q0 TXPLL0	No	No	3GHz +1.4dB	200mV with 0dB	8b/10b	32	No	0.000	0.000	0.000	0.000
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	Duplex					Q0 TXPLL0	No	No	3GHz +1.4dB	200mV with 0dB	8b/10b	32	No	0.000	0.000	0.000	0.000
	Duplex					Q0 TXPLL0	No	No	3GHz +1.4dB	200mV with 0dB	8b/10b	32	No	0.000	0.000	0.000	0.000
	Duplex					Q0 TXPLL0	No	No	3GHz +1.4dB	200mV with 0dB	8b/10b	32	No	0.000	0.000	0.000	0.000
	Duplex					Q0 TXPLL0	No	No	3GHz +1.4dB	200mV with 0dB	8b/10b	32	No	0.000	0.000	0.000	0.000
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	Duplex					Q0 TXPLL0	No	No	3GHz +1.4dB	200mV with 0dB	8b/10b	32	No	0.000	0.000	0.000	0.000
	Duplex					Q0 TXPLL0	No	No	3GHz +1.4dB	200mV with 0dB	8b/10b	32	No	0.000	0.000	0.000	0.000
	Duplex					Q0 TXPLL0	No										

PLL & DLLの設定

- “PLL & DLL”シートで入力

- PLLやクロックシステムを個別の名称で、入力周波数/出力周波数/Modeを設定

Return to Summary

PLL and DLL Power

Rail	Voltage (V)	Power (W)
VDD	1.000	0.002
VDD25	2.500	0.002
Total Power		0.004

0% of total power 1.875 W

Resource	Power (W)
PLL	0.004
DLL	0.000

Utilization	Count	Percentage
PLL	2	25%
DLL	0	0%

[Clocking Resources User Guide](#)

[MPE User Guide](#)

PLL Power

Name	Reference Clock Frequency (MHz)	Output 0 Frequency (MHz)	Output 1 Frequency (MHz)	Output 2 Frequency (MHz)	Output 3 Frequency (MHz)	Mode	VDD Power (W)	VDD25 Power (W)
PF_CCC_C0	125	125				Min VCO for Low Power	0.001	0.001
PF_CCC_C1	148.5	148.5				Min VCO for Low Power	0.001	0.001
						Min VCO for Low Power	0.000	0.000
						Min VCO for Low Power	0.000	0.000
						Min VCO for Low Power	0.000	0.000
						Min VCO for Low Power	0.000	0.000
						Min VCO for Low Power	0.000	0.000
						Min VCO for Low Power	0.000	0.000

DLL Power

Name	Reference Clock Frequency (MHz)	VDD Power (W)
		0.000
		0.000
		0.000
		0.000
		0.000
		0.000
		0.000
		0.000
		0.000

Navigation: ... Clock Logic LSRAM uSRAM Math Block IO Transceiver **PLL & DLL** User Release

結果の確認

- “Summary”で結果を確認

The screenshot displays the Microchip Power Estimator (MPE) v2021.2 interface for PolarFire and PolarFire SoC. The interface includes a top navigation bar with the Microchip logo and title, a toolbar with buttons for Import, Initialize Power Estimator, Manage IP, Create Snapshot, Reset to Defaults, and Export Report, and a Project field. The main area is divided into Settings and Power Summary sections.

Settings - General

Family	PolarFire
Device	MPF300T
Package	FCG484
Range	Extended
Core Voltage	1.0 V
Process	Typical
Speed Grade	STD
Data State	Production

Power Summary

Summary		
Total Power (W)	2.189	
→ Device Static (W)	0.107	
→ Core Dynamic (W)	2.079	
→ I/O (W)	0.003	
→ Transceiver (W)	0.000	
Junction Temperature T _J (-C)	25.00	
Effective Theta JA (-C/W)	N/A	
Thermal Margin	Maximum Ta (-C)	N/A
	Maximum Power (W)	N/A

The "Summary" tab in the bottom navigation bar is highlighted with a red box.

使用方法3

macnica

使用方法3

- **Libero SoC からのImport**

- Libero SoC にて設計中でPlace & Routeまで可能、または、PLLやIPを配置済みでPlace & Routeまで可能なサンプルデザインが用意可能

- **注意**

- MPEとLibero SoCのバージョンは要確認

Libero SoC のSmartPower で生成

● MPE のImport用ファイルの出力

- SmartPower 起動後“Tools” => “Export Report for MPE...” を選択

The screenshot shows the SmartPower application window. The 'Tools' menu is open, and 'Export Report for MPE...' is highlighted. The main window displays a 'Power Usage' pie chart with the following data:

Category	Value
Total	52.185 mW
Static	52.185 mW
Dynamic	0 mW

The pie chart shows 'Core Static' at 51.735 mW and 'Other Rails Static' at 0.45 mW. Below the chart is a table of operating conditions:

Operating Conditions	Value
1 Junction Temperature	25 C
2 Process	Typical
3 VDD	1 V
4 VDDAUX	2.5 V
5 VDDI 3.3	3.3 V
6 VDD25	2.5 V
7 VDD18	1.8 V

At the bottom, there are fields for 'Battery capacity' (1000.00 mAh) and 'Battery Life' (22479 Hour(s)).

Import

- “Summary”シートの“Import”を選択

The screenshot displays the Microchip Power Estimator (MPE) v2021.2 interface for PolarFire and PolarFire SoC. The 'Import' button is highlighted with a red box. The interface is divided into two main sections: 'Settings' and 'Power Summary'.

Settings - General

Family	PolarFire
Device	MPF300T
Package	FCG484
Range	Extended
Core Voltage	1.0 V
Process	Typical
Speed Grade	STD
Data State	Production

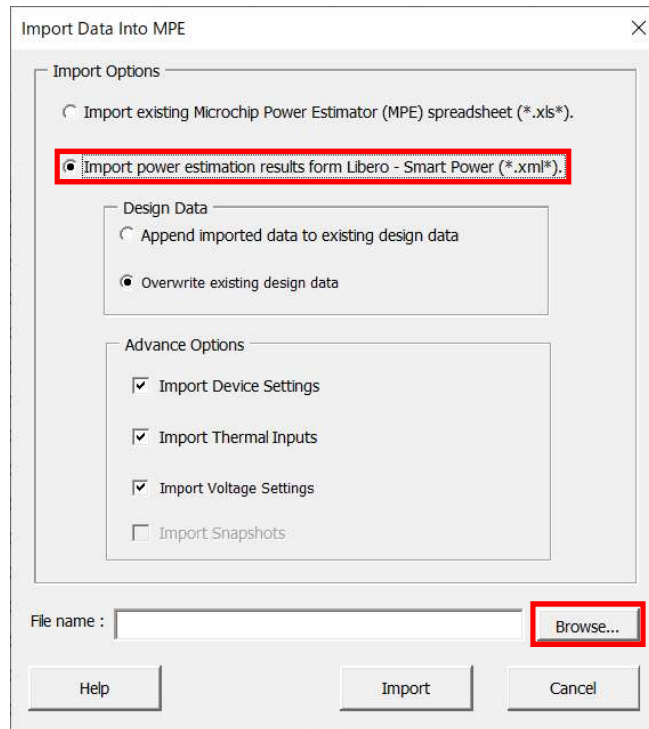
Power Summary - Summary

Total Power (W)	0.917	
→ Device Static (W)	0.102	
→ Core Dynamic (W)	0.813	
→ I/O (W)	0.002	
→ Transceiver (W)	0.000	
Junction Temperature T _J (-C)	25.00	
Effective Theta JA (-C/W)	N/A	
Thermal Margin	Maximum Ta (-C)	N/A
	Maximum Power (W)	N/A

The bottom of the interface shows a navigation bar with tabs for Summary, Graphs, Snapshot, Current Breakdown, Clock, Logic, LSRAM, uSRAM, Math Block, IO, Transceiver, PLL & DLL, User, and Release. The 'Summary' tab is currently selected.

Import

- “Import power estimation results form Libero – Smart Power (*.xml)”を選択
- “Brows…”からSmartPowerよりExportしたファイルを選択



結果の確認

- “Summary”で結果を確認

The screenshot displays the Microchip Power Estimator (MPE) v2021.2 interface for PolarFire and PolarFire SoC. The interface includes a top navigation bar with buttons for Import, Initialize Power Estimator, Manage IP, Create Snapshot, Reset to Defaults, and Export Report. Below this is a Project field and a Settings section with a General tab. The Power Summary table is highlighted with a red border and contains the following data:

Summary		
Total Power (W)		2.189
→ Device Static (W)		0.107
→ Core Dynamic (W)		2.079
→ I/O (W)		0.003
→ Transceiver (W)		0.000
Junction Temperature T _J (-C)		25.00
Effective Theta JA (-C/W)		N/A
Thermal Margin	Maximum Ta (-C)	N/A
	Maximum Power (W)	N/A

履歴

● 改版

リビジョン	日付	概要
V2021_R1.0	2022年4月	新規作成

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