HyperLynx SI 機能比較表（VX2.10）

項目	内容	DDRx	GH z Bundle	項目数
Configuration	Application product	○		**3**
	Bundle product		○	
	Station product			
項目	**内容**	**DDRx**	**GH z Bundle**	**項目数**
Licensing	Perpetual	○	○	**4**
	Short-term lease	○	○	
	Termination Check	○	○	
	Term w/remix	○	○	
項目	**内容**	**DDRx**	**GH z Bundle**	
Environment	Pre-layout	○	○	**5**
	Post-layout	○	○	
	Interface to 3rd-party PCB flow / PCB translators	○	○	
	Integrated with CES	○	○	
	Analysis integrated within Xpedition (XAC)			
項目	**内容**	**DDRx**	**GH z Bundle**	
Signal Integrity	Basic IBIS simulation, Stackup Editing, EMC, Multiboard, Loss and Crosstalk	○	○	**25**
	Import/use S-parameter models in simulations	○	○	
	DDRx wizard: integrated SI / timing verification	○	○	
	DDR, DDR2, DDR3, LPDDR, LPDDR2 and LPDDR3	○	○	
	DDR4 and LPDDR4	○	○	
	NV-DDR2 and NV-DDR3	○	○	
	DDR5 and LPDDR5 with IBIS-AMI models	○	○	
	Advanced DDRx AMI (support for asymmetric single-ended I/O)	○	○	
	Pulse response simulation (model-free)	○	○	
	Stacked die/MCM Electrical Module Description (EMD) support	○	○	
	EZWave waveform display	○	○	
	Supports SPICE / ADMS simulation engines		○	
	SerDes analysis		○	
	SerDes Compliance Wizard with support for over 180 standard protocols		○	
	Post-layout SerDes extraction (requires HLAS P/N 266125 or 268014)		○	
	Automated identification / modeling of 3D areas (requires FWS or HPC license)		○	
	IBIS-AMI simulation support		○	
	FastEye simulation (SerDes channel simulation without IBIS-AMI models)		○	
	Support for via backdrilling, surface roughness trace modeling		○	
	S-parameter generation, Touchstone Viewer, metrics		○	
	Integrated 3D EM via modeling for simple via configurations		○	
	Power-Aware (Non-ideal return path & SSN) simulation option, includes:	Option	Option	
	Hybrid 3D EM solver	-	-	
	PDN & via extraction (single and diff via)	-	-	
	SI & plane co-simulation	-	-	