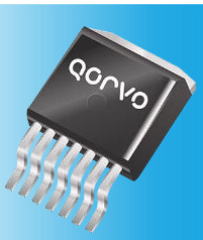
APPLICATION NOTE

Qorvo Surface Mount Technology Devices

By Jonathan Dodge, P.E.

Introduction

Pick-and-place machines place surface mount technology (SMT) devices on a circuit board very quickly and with excellent precision. This ability combined with a highly repeatable solder process in a reflow oven results in low assembly cost with superior mechanical reliability. These benefits are further enhanced by reduced stray inductance and package resistance (better electrical and EMI performance) in SMT power devices. The use of SMT power devices is enabled in part by the low power loss of SiC devices.This application note addresses the construction, land patterns, moisture sensitivity level and reflow solder profile for Qorvo SMT devices.



Qorvo SMT products combine the benefits of highly repeatable, low-cost manufacturing processes with excellent electrical performance.

Scope

This document provides package, land pattern, solder profile and storage information for Qorvo surface-mount technology (SMT) devices, including D2PAK-7L (TO-263-7L), D2PAK-3L (TO-263-3L), and TOLL (MO-229).

Qorvo SMT Construction

Qorvo SMT devices are constructed with a 100% matte tin-plated copper lead-frame and pins, as shown in a cross-section drawing of a (TO-263-7L) below in **Figure 1**. The D2PAK-3L and other SMT device constructions are similar. The exposed metal on the bottom side of the package, referred to as the tab, is always the electrical connection to the drain.

Most Qorvo SMT products use silver-sintered connections that maintain integrity at temperatures of several hundred degrees C, and consequently have no concern of re-melting sintered connections during PCB assembly or rework processes. A further advantage of silver sintering versus solder is significantly reduced thermal resistance between the chip and the copper lead-frame, which results in a lower junction-case thermal resistance. The few SMT products with solder-attached chips use high-lead content, high-temperature solder that melts at 380°C.

All of Qorvo's SiC products are RoHS compliant, even those that use solder instead of sintering. Use of lead in high-melting-temperature solder is allowed by the RoHS initiative.

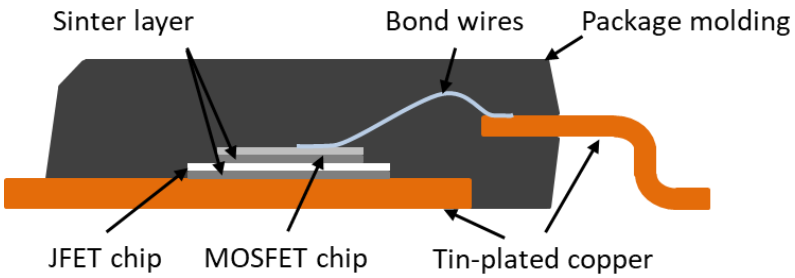


Figure 1. D2PAK-7L cross-section drawing of a Qorvo cascode. (not to scale, JFET gate bond wire omitted for clarity).

Package	D2PAK-3L	D2PAK-7L	TOLL
Voltage rating	≤ 750V	≤ 2000V	≤ 750V
Max Id rating	<75A	<150A	<200A
Cu thickness	1.3mm	1.3mm	0.5mm
Package size	10x15mm	10.2x15.5mm	9.9x11.3mm
Package height	4.5mm	4.5mm	2.3mm
Thermal die pad	7.6x7.2mm	4.8x9.1mm	6.9x8.1mm
Inductance, source+drain	<5nH	<3nH	<2nH
Creepage	0.92mm	6.66mm	2.8mm
Clearance	0.92mm	6.09mm	2.8mm
Kelvin source	No	Yes	Yes

Table 1: Surface mount packages' mechanical details.

Cascode

The cascode construction is either stacked or side-by-side. The cross-section drawing of Figure 1 is that of a stacked cascode with the chip silver sintered to the copper lead-frame, and the low-voltage MOSFET chip sintered directly on top of the JFET chip. The stacked cascode has the designation 'SC' in the part number, such as UJ4SC075011B7S. The letter 'S' at the end of the part number designates silver sinter chip attach. If this final 'S' is missing, then the chip attach is with high-temperature solder.

FET-Jet CALCULATOR

Qorvo's SiC SMT products are included in FET-Jet Calculator

In the side-by-side construction, the low-voltage MOSFET is mounted on a ceramic substrate. The ceramic substrate is often referred to as DBC, which stands for the direct bonded copper, with the top-side copper forming a printed circuit pattern. The side-by-side configuration has only the letter 'C' following the Generation designator, such as UJ4C075033B7S. As with the stacked configuration, the letter 'S' at the end of the part number designates silver sinter chip attach; or high-temperature solder without it.

JFET

JFET products of course have only the JFET chip inside the package; the MOSFET chip in Figure 1 is omitted, and wires are bonded to the top of the JFET chip. As with cascode part numbers, the inclusion or omission of the letter 'S' at the end of the part number designates silver sinter or high-temperature solder chip attach, respectively.

Package Outline Drawings and Printed Circuit Board Land Patterns

Following are package outline drawings (POD) and PCB land patterns for various SMT packages. Land pattern refers to the metal pads on the PCB surface where solder paste is applied. Footprint refers to the package outline as viewed from above.

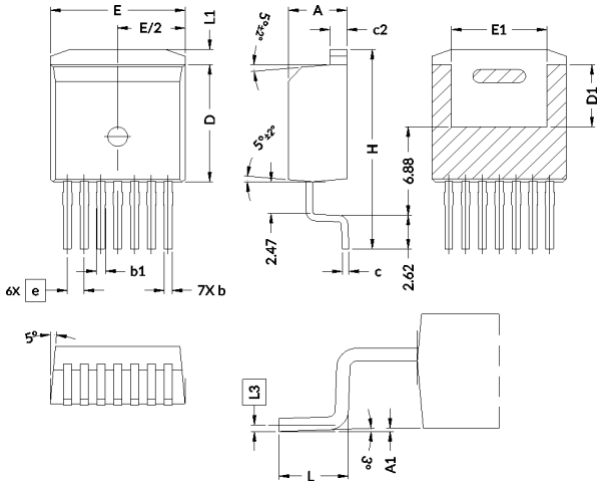


Figure 2. D2PAK-7L (TO-263-7L) package outline drawing.

D2PAK-7L						
Sym	mm			Inch		
	Min	Nom	Max	Min	Nom	Max
A	4.30	4.43	4.56	0.169	0.174	0.180
A1	0.00	0.13	0.25	0.000	0.005	0.010
b	0.50	0.60	0.70	0.20	0.024	0.028
b1	0.60	0.70	0.90	0.024	0.028	0.035
c	0.50 BSC			0.020 BSC		
c2	1.20	1.30	1.40	0.047	0.051	0.055
D	8.93	9.08	9.23	0.352	0.357	0.363
D1	4.65	4.80	4.95	0.183	0.189	0.195
e	1.27 BSC			0.050 BSC		
E	10.08	10.18	10.28	0.397	0.401	0.405
E1	6.82	7.22	7.62	0.269	0.284	0.300
H	15.00	15.50	16.00	0.591	0.610	0.630
L	1.90	2.20	2.50	0.075	0.087	0.098
L1	0.98	1.20	1.42	0.039	0.047	0.56
L3	0.25 BSC			0.010 BSC		

Table 2. D2PAK-7L (TO-263-7L) package outline drawing dimensions table.

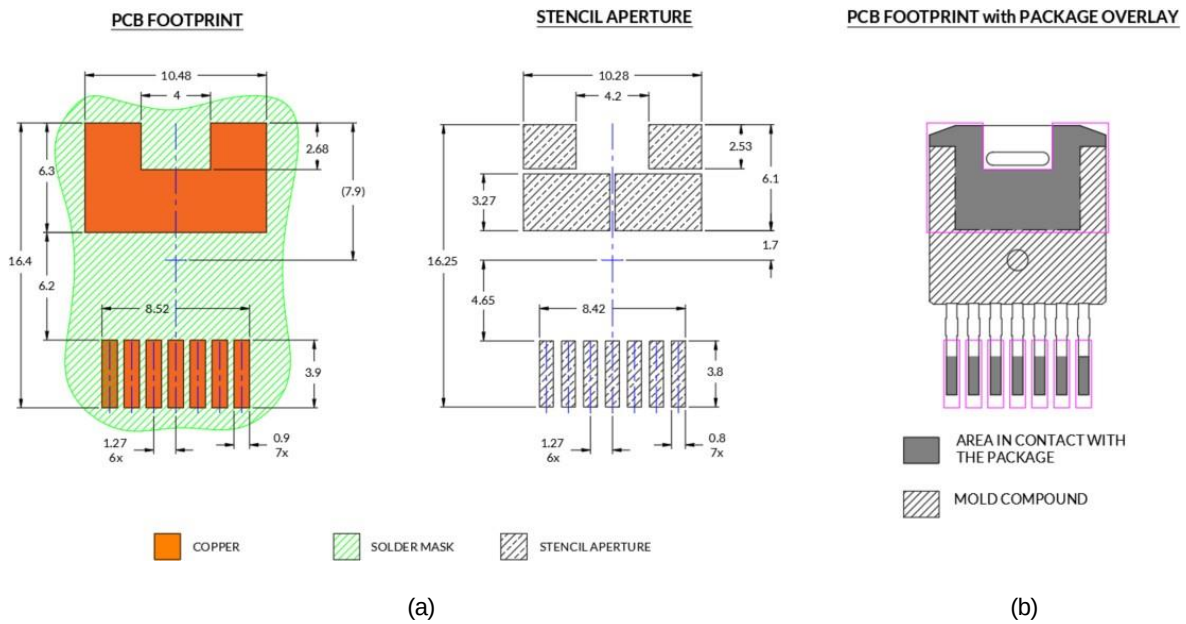


Figure 3. D2PAK-7L (a) PCB land pattern with dimensions in millimeters,
(b) footprint overlaying land pattern highlighting area within land pattern in contact with package metal.

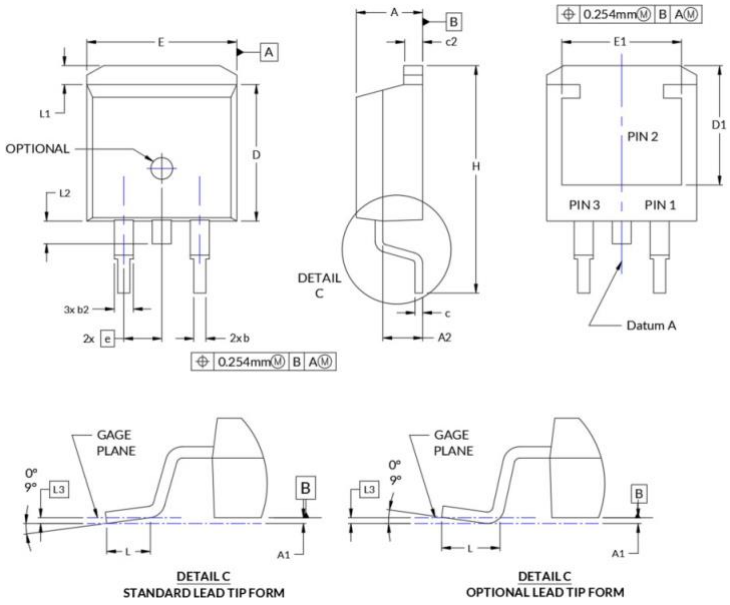


Figure 4. D2PAK-3L (TO-263-3L) package outline drawing.

D2PAK-3L						
Sym	mm			Inch		
	Min	Nom	Max	Min	Nom	Max
A	4.06	4.45	4.83	0.160	0.175	0.190
A1	0.00	–	0.25	0.000	–	0.010
A2	2.20	2.67	2.90	0.087	0.105	0.114
b	0.51	0.81	0.99	0.020	0.032	0.039
b2	1.14	1.27	1.78	0.045	0.050	0.070
c	0.38	0.50	0.74	0.015	0.020	0.029
c2	1.14	1.27	1.65	0.045	0.050	0.065
D	8.38	9.14	9.65	0.330	0.360	0.380
D1	6.86	8.00	8.37	0.270	0.315	0.330
e	2.54 BSC			0.100 BSC		
E	9.65	10.03	10.67	0.380	0.395	0.420
E1	6.22	8.00	8.37	0.245	0.315	0.330
H	14.61	15.24	15.88	0.575	0.600	0.625
L	1.78	2.54	2.79	0.070	0.100	0.110
L1	1.02	1.27	1.68	0.040	0.050	0.066
L2	1.27	1.52	1.78	0.050	0.060	0.070
L3	0.25 BSC			0.010 BSC		

Notes:
1. Controlling dimension: Millimeters
2. Package body sides does not include mold flash and gate burrs
3. Dimension L is measured in gage line
4. Converted inch dimensions are not necessarily exact
5. Package marking: refer to DS_TO_263_3L

Pin Designations:
Pin 1: Source
Pin 2: Drain
Pin 3: Gate

Table 3. D2PAK-73 (TO-263-3L) package outline drawing dimensions table.

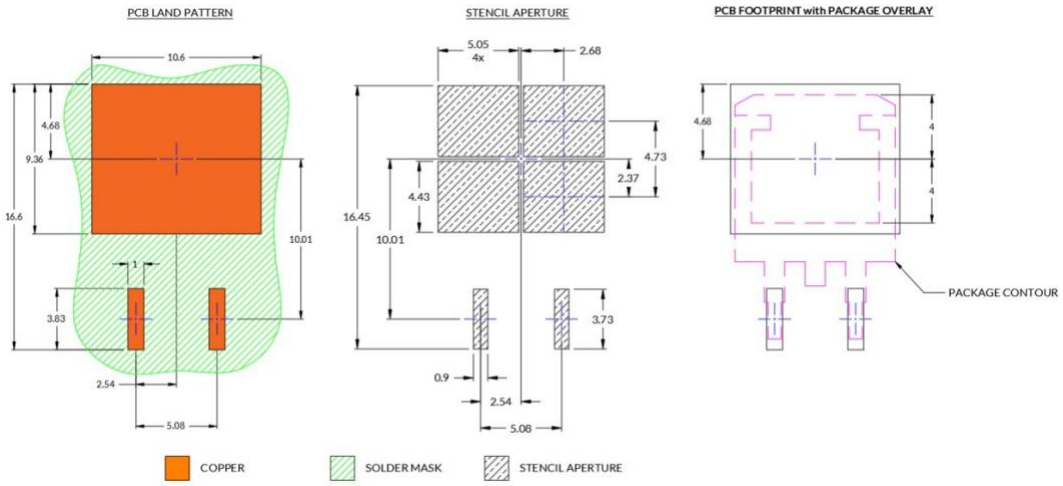
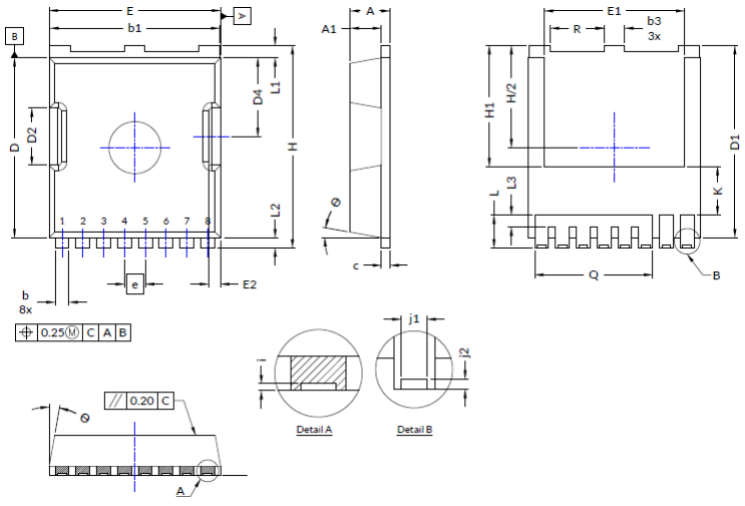


Figure 5. D2PAK-3L PCB land pattern with dimensions in millimeters.



Notes:
1. All dimensions in millimeters
2. Dimensions do not include burrs and mold flashes
3. Dimensions in compliance with JEDEC MO-2998B except for backside heatsink exposed pad dimention, E1 and H1

Pin Designations:
1. Gate
2. Source Kelvin

Figure 6. TOLL (MO-229) package outline drawing.

TOLL			
Sym	mm		
	Min	Nom	Max
A	2.15	2.30	2.45
A1		1.80 REF	
b	0.70	0.80	0.90
b1	9.65	9.80	9.95
b3	1.10	1.20	1.30
c	0.40	0.50	0.60
D	10.18	10.38	10.58
D1	10.98	11.08	11.18
D2	3.15	3.30	3.45
D4	4.40	4.55	4.70
E	9.70	9.90	10.10
E1	7.95	8.10	8.25
E2	0.60	0.70	0.80
e		1.20 BSC	
H	11.48	11.68	11.88
H1	6.80	6.95	7.10
i		0.10 REF	
j1		0.46 REF	
j2		0.20 REF	
K		2.80 REF	
L	1.40	1.90	2.10
L1	0.50	0.70	0.90
L2	0.48	0.60	0.72
L3	0.30	0.70	0.80
Q		6.80 REF	
R	3.00	3.10	3.20
θ		10°	

Table 4. TOLL POD dimensions.

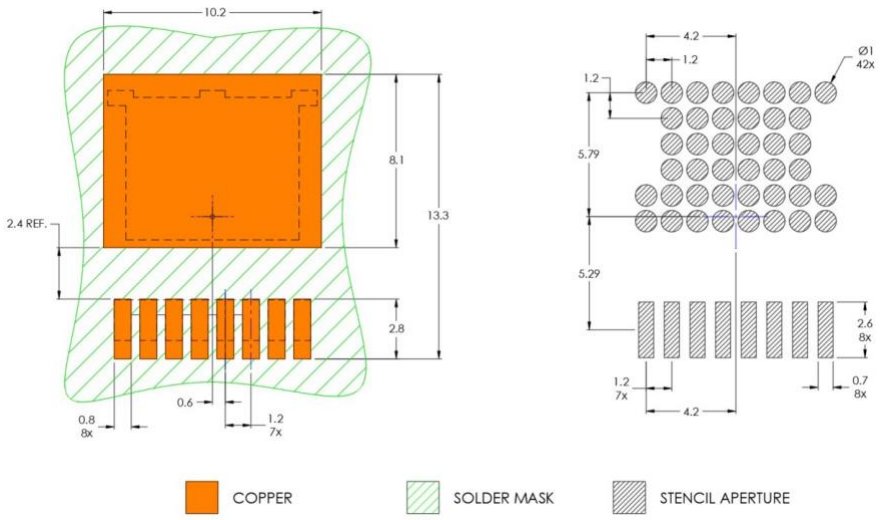


Figure 7. TOLL land pattern with dimensions.

Moisture Sensitivity Level (MSL)

The expansion of trapped moisture can damage SMT components during rapid temperature changes in the solder reflow process. Such damage is often not visible, but in severe cases can result in bulges or external cracks. Moisture sensitivity level (MSL) is based on JEDEC standard J-STD-020 with the purpose of defining levels corresponding to proper packaging, storage and handling to avoid damage. The MSL standard specifies the period for which a moisture-sensitive device can be exposed to ambient room conditions before going through a reflow or rapid temperature-change rework process.

MSL	Qorvo Parts	Floor Life	Relative Humidity
1	All D2PAK-3L	Unlimited	85%
2		1 year	60%
2a		4 weeks	
3	D2PAK-7L, TOLL	168 hours	
4		72 hours	
5		48 hours	
5a		24 hours	
6		Time on label (TOL) after bake	

Table 5. MSL levels and floor life at 30 °C.

Floor life refers to the time after product is removed from its sealed, dry, packing. Higher temperature and/or higher humidity increases moisture absorption in the SMT package and shortens the floor life. Conversely, lower temperature and/or lower humidity generally reduces moisture ingress and therefore increases the floor life.

Products that exceed their floor life can be baked dry and then run through the solder reflow process. Also, products with MSL rating of 2 or higher (more moisture sensitive) may need to be baked before certain types of rework. Refer to JEDEC standard J-STD-033 for bake conditions and time.

All Qorvo SiC products in the D2PAK-3L package are MSL1. Products in D2PAK-7L and TOLL are MSL3. Gen 3 includes cascode FETs and JFETs with part numbers that begin with UJ3 or UF3.

Reflow Profile

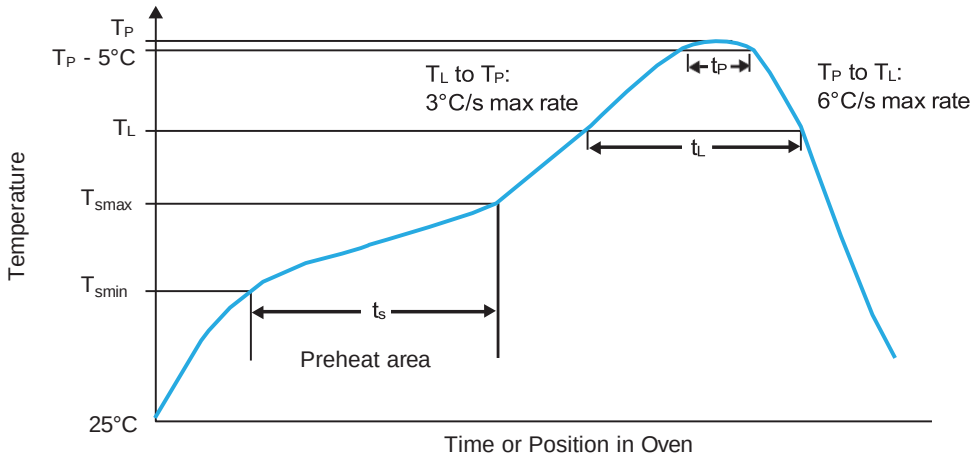


Figure 8. Reflow profile, referred to as Classification Profile in J-STD-020.

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (t_s) from T_{smin} to T_{smax}	 100°C 150°C 60-120 seconds	 150°C 200°C 60-120 seconds
Ramp-up rate (T_L to T_P)	3°C/second maximum	
Liquidous temperature (T_L) Time (t_L) maintained above T_L	183°C 60-150 seconds	217°C 60-150 seconds
Classification temperature (T_C)	D2PAK-3L: 220°C D2PAK-7L: 220°C TOLL: 235°C	D2PAK-3L: 245°C D2PAK-7L: 245°C TOLL: 260°C
Time (t_P)* within 5°C of T_C, see Figure 8	20 seconds	30 seconds
Time 25°C to peak temperature	6 minutes max.	8 minutes max.

Table 6. Classification profiles.

The classification temperature (T_C) in is the maximum allowed peak temperature (T_P), which is measured at the top of the package.

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About the Author

Jonathan Dodge is the Principal Applications Engineer at Qorvo. His experience includes design of analog, digital and power electronics; working with power levels ranging from 1.5 to 500 kW in renewable energy and other applications.