

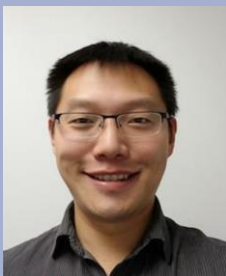
APPLICATION NOTE
UnitedSiC_AN0024 - August 2020

How to slow down dV/dt during switching

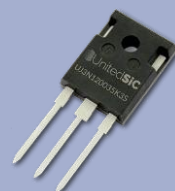
By Dr Zhongda Li, Senior Staff R&D Engineer, UnitedSiC.

Introduction

For certain applications, such as motor control, it is important to slow dV/dt down during switching. Too fast and it would cause a high voltage spike on the motor, which could damage the winding insulation and so, reduce motor life. In this app note, Zhongda Li from UnitedSiC, compares three different dV/dt control methods.



Dr. Zhongda Li received his B.S in Physics from Peking University in 2007, and Ph.D in Electrical Engineering from Rensselaer Polytechnic Institute in 2013. He has over 10 years' research experience in SiC and GaN device technologies. He has published more than 30 technical papers and holds 4 US patents.



Learn more about power electronic applications at <https://unitedsic.com/downloads>

dV/dt switching

The conventional method for reducing switching dV/dt of silicon MOSFETs, IGBTs and SiC MOSFETs would be increasing the external gate resistor value. Because these devices have relatively high CGD (CRSS), external RG values can slow down dV/dt without excessive delay times. This method is great for fast switching applications, such as Totem-pole PFC, where faster dV/dt leads to lower switching loss. However, for slower applications, such as a motor, it would require a very high resistance value. To slow it down to 5~8V/ns would require a gate resistance of several kilo-Ohms, which would result in excessively long switching delay time and therefore a low stepping rate. For position control applications, this would be detrimental to performance.

There are methods that can effectively control dV/dt of SiC FET devices from 45V/ns to 5V/ns, without the penalty of excessive delay time. The three methods are: external gate drain capacitor, device RC-snubber and JFET direct drive, using a UnitedSiC 9mΩ 1200V SiC FET in a standard TO247-4L package (UF3SC120009K4S¹), switched at 75A/800V.

External gate drain capacitor

The first method is to add an external gate drain capacitor (CGD) between gate and drain of both high side and low side FETs of a half-bridge. For chosen SiC FET, the value of CGD_{EXT} has been selected to be 68pF. A 20nH parasitic inductance was deliberately added in series with external capacitor, to illustrate that this method is not sensitive to parasitic inductances in its path (Figure. 1).

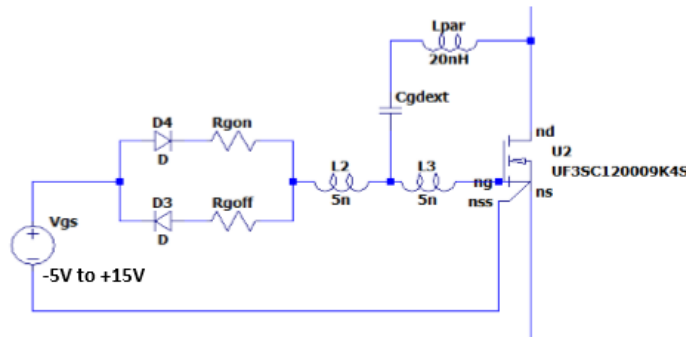


Figure 1 Gate drive with external CGD (on both high side and low side FET) for dV/dt control

In real applications, where discretés are used, this parasitic inductance should be much less than 20nH, since the external CGD can be placed close to the FETs on PCB. However, if the UnitedSiC FET chips are used inside modules with the external CGD placed outside the module, it could be possible to have 20nH parasitic inductance in its path.

¹ UF3SC120009K4S detail: <https://unitedsic.com/products/sic-fets/uf3sc120009k4s/>

The external CGD method was first optimized with SPICE simulations, using the UF3SC120009K4S SPICE model²³, then verified experimentally using a double pulse testing circuit. The 68pF external CGD was soldered deliberately between the G and D leads of the TO247-4L, instead of on the PCB board, to increase parasitic inductance in its path.

Turn-off and turn-on waveforms from the experimental measurement and SPICE simulation were overlaid for comparison. In **Figure 2**, the measured and simulated waveforms matched very well.

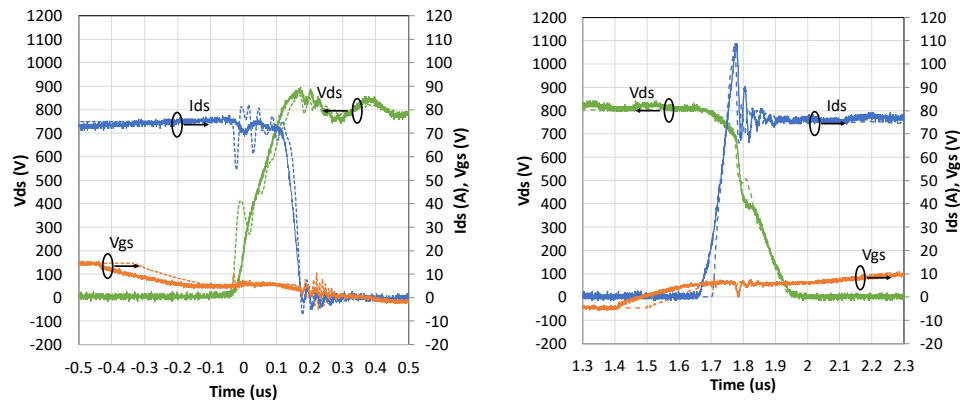


Fig 2 Overlaid turn-off (left) and turn-on waveforms of experimental (solid lines) and SPICE simulation (dash lines), 75A 800V external CGD 68pF and RG 33Ω

With the 68pF external CGD, dV/dt was effectively controlled in the range of 25V/ns to 5V/ns, using RG of 10Ω to 33Ω. For both SPICE and experiment, EON and EOFF were extracted by integrating $I_{DS} \times V_{DS}$ during turn-on and turn-off transition, which increased with RG as expected.

The reason why the external CGD can tolerate high parasitic inductance (20nH in SPICE) was that the current was quite low during switching. For an external CGD of 68pF and dV/dt of 8V/ns, the estimated current was only 0.54A and was consistent with the current from SPICE simulations. This is, therefore, applicable to modules, where the external CGD is placed outside the module on the gate drive PCB, with some parasitic inductance in its path.

Device RC-Snubber

The second dV/dt control method adds RC snubbers in parallel to the switches for both high side and low side. A 20nH parasitic inductance was deliberately added in series with the snubber, for the purpose of proving this method can tolerate parasitic inductance in the snubber path (**Figure 3**).

² Zhongda Li: Importing UnitedSiC Models into LTSPICE, Application Note: <https://unitedsic.com/appnotes/AN0005-Using%20UnitedSiC%20SPICE%20model%20in%20LTSPICE.pdf>

³ Mike Zhu: Switching Fast SiC FETs with a Snubber, Application Note: https://unitedsic.com/appnotes/Snubber%20AppNotes_V8.pdf

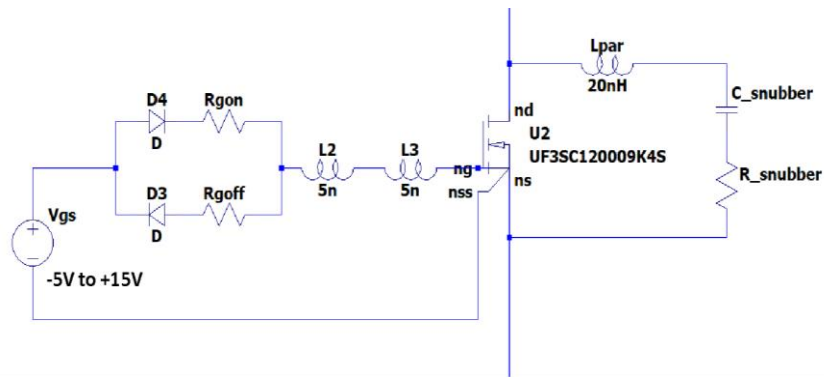


Fig 3 RC snubber parallel to FET (on both high side and low side FET) for dV/dt control

In real applications, when using discretes, the RC snubber can be placed very close to the FET, and the parasitic inductance would be only a few nH. But if the UnitedSiC FET chips are used inside modules, the RC snubber can be placed outside the module, and it is possible to have 20nH parasitic inductance in its path.

Turn-off and turn-on waveforms from experimental measurement and SPICE simulation were overlaid for comparison (Figure 4). Note that the I_{DS} current in the plots included the snubber current. Experimental and SPICE showed dV/dt can be effectively controlled from 50V/ns to 5V/ns by $C_{SNUBBER}$ (snubber capacitor) up to 5.6nF.

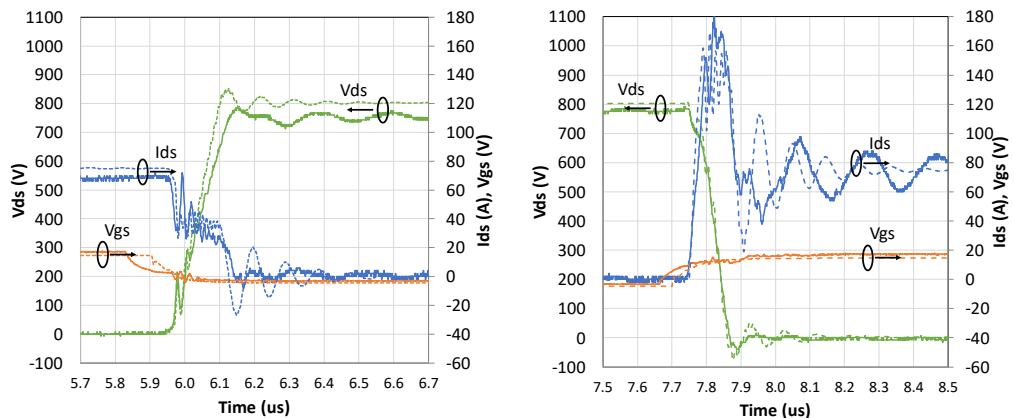


Fig 4 Overlaid turn-off (left) and turn-on waveforms of experimental (solid lines) and SPICE simulation (dash lines), 75A 800V with RC snubber 0.5Ω 5.6nF

The switching losses (EON, EOFF and ESW) were extracted by integrating $I_{DS} \times V_{DS}$ during the switching transitions, where I_{DS} included the snubber current. Therefore, the EON and EOFF included the losses on the snubbers. However, the snubber loss on the 0.5Ω $R_{SNUBBER}$ was very low, especially at slower dV/dt . With a $C_{SNUBBER}$ of 4nF and turn-off $dV/dt=8V/ns$, SPICE showed that the snubber loss was only 0.2mJ, or 2W for $f=10kHz$ switching. It is found that the snubber can also tolerate high parasitic inductance (20nH in SPICE), and therefore in the case of modules the RC snubber can be placed outside module.

JFET direct drive

The third method is direct drive, where the Si MOS is turned on only once at circuit start up, and JFET gate is switched directly between -15V to 0V (Figure 5). In this configuration, normally-off operation is preserved, however, the gate PWM and simple Enable signals would be required.

The high side JFET is kept off by -15V during switching transients, and synchronous rectification is necessary for freewheeling JFET to reduce its conduction loss in the third quadrant.

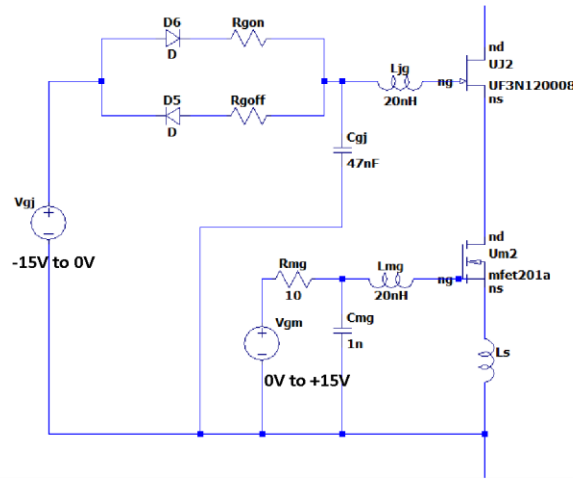


Fig 5 JFET Direct drive method (on both high side and low side FET) for dV/dt control

Because the SiC JFET has considerable CRSS (C_{GD}), a small RG of 4.7Ω would be enough to slow down dV/dt to 5V/ns. Turn-off and turn-on waveforms from experimental measurement and SPICE simulation were overlaid for comparison (Figure 6).

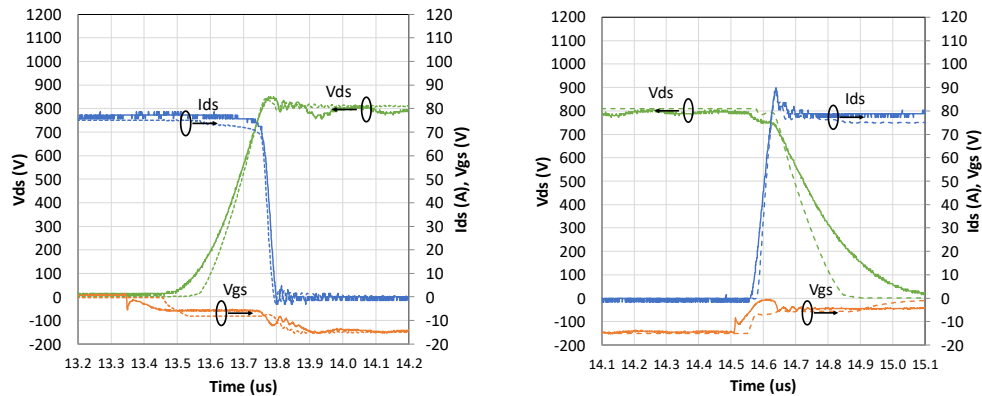


Fig 6 Overlaid turn-off (left) and turn-on waveforms of experimental (solid lines) and SPICE simulation (dash lines), 75A 800V, JFET direct drive with RG 4.7Ω

The IDS current waveforms matched well between SPICE (dash lines) and experimental waveforms (solid lines). But the experimental VDS waveforms showed slower dV/dt than the SPICE waveform. The reason could be that the JFET gate driver used in the experiment was not able to provide enough gate current to charge or discharge the JFET CRSS during the dV/dt transition, causing it to be slowed down.

The resulting dV/dt from SPICE and measurement were compared, showing dV/dt can be well controlled from 15V/ns to 4V/ns. The switching losses were extracted using the same way as the previous methods, and EON and EOFF increased with JFET RG as expected.

Comparison of the three dV/dt control methods

The three methods were compared using SPICE simulations under the same limitation of $dV/dt \leq 8V/ns$ (Table 1).

Table 1 Comparison of SPICE simulated performance of 75A/800V switching with maximum $dV/dt=8V/ns$

Method	Gate Drive Condition	JFET Gate Access Needed	dV/dt _{off} (V/ns)	dV/dt _{on} (V/ns)	di/dt _{on} (A/ns)	Vds Peak, low side (V)	Vds Peak, high side (V)	E _{off} (mJ)	E _{on} (mJ)	E _{sw} (mJ)
External Cgd	External Cgd=68pF, Rgon=18 ohm, Rgoff=22.1 ohm Vgon=+15V, Vgoff=-5V	No	8.0	8.0	4.1	881	853	5.56	5.26	10.82
Snubber	Csn=8.2nF, Rsn=0.5ohm, Rgon=5 ohm, Rgoff=5 ohm, Vgon=+15V, Vgoff=-5V	No	4.0	8.0	5.5	842	902	2.99	7.17	10.17
Direct Drive	JFET Rgon=1.05 ohm, JFET Rgoff=1.65 ohm, JFET Vgon=0V, JFET Vgoff=- 15V, Si MOS Vg=15V (stay on)	Yes	8.0	8.0	4.09	862	806	3.47	5.55	9.02

The JFET direct drive method showed the lowest overall switching loss of 9.02mJ. Compared with the other two methods, this method required negative voltage for driving the SiC JFET, as well as an enable signal for the Si MOS at circuit start up, adding some complexity to the gate drive. The standard UnitedSiC FETs do not provide access to the JFET gate, but a new dual-gate TO247-4L product is under development, which has both SiC JFET gate and Si MOS gate and would be suitable for JFET direct drive. This method would also be suitable for modules, where a separate JFET gate pin can be added. As shown in this study, the JFET gate path can tolerate reasonable amount of parasitic inductance (20nH in SPICE), so it would be feasible to have the JFET gate driver placed on the gate drive PCB board that is on top of the module.

The external CGD and device RC snubber methods showed higher switching loss, but they did not require access to the JFET gate. Both methods can be easily implemented on the PCB, when using UnitedSiC FETs in discrete packages (e.g. TO247). Since both methods can tolerate a reasonable amount of parasitic inductance (20nH in SPICE), they would also be suitable for modules with UnitedSiC chips inside.

One drawback of the RC snubber method was that it cannot adjust turn-off and turn-on dV/dt independently. As shown in Table 1, to achieve turn-on dV/dt of 8V/ns, the turn-off dV/dt had to be reduced to 4V/ns, which increased EOFF.

However, they can be adjusted independently using a separate RGON and RGOFF for external CGD and JFET direct drive methods. As shown in Table 1, turn-off and turn-on dV/dt of 8V/ns was achieved by optimizing RGON and RGOFF separately.

Summary

In summary, with these simple techniques, good dV/dt control can be achieved. The UnitedSiC FET advantages of lower conduction loss and good short-circuit robustness are paramount to efficient and reliable motor drive applications.

References

- [1] A. Binder, "High frequency effects in inverter-fed AC electric machinery", ICEM2016 tutorial: www.ew.tu-darmstadt.de/media/ew/vortrge/ICEM2016_Tutorial_HighFrequencyEffects_Binder_final.pdf
- [2] Link to UF3SC120009K4S detail: <https://unitedsic.com/products/sic-fets/uf3sc120009k4s/>

- [3] Zhongda Li: Importing UnitedSiC Models into LTSPICE, Application Note:
<https://unitedsic.com/appnotes/AN0005-Using%20UnitedSiC%20SPICE%20model%20in%20LTSPICE.pdf>
- [4] Mike Zhu: Switching Fast SiC FETs with a Snubber, Application Note:
https://unitedsic.com/appnotes/Snubber%20AppNotes_V8.pdf