Cascode Configuration Eases Challenges of Applying SiC JFETs

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Abstract

The high switching speeds and low $R_{DS(ON)}$ of high-voltage SiC JFETs can significantly improve the efficiency and power density of many power conversion applications. However, the conventional view of these devices is that, despite the parametric advantages, JFETs are difficult to implement due to non-standard drive voltages and a lack of an intrinsic diode when switching inductive loads.

This article describes the use of a JFET in cascode to solve both of these issues by utilizing the intrinsic diode and the drive voltages of a standard low-voltage MOSFET. It will also highlight the general robustness of SiC JFETs in cascode with respect to short circuit and avalanche conditions.

After explaining the basic operation of a SiC JFET plus silicon MOSFET cascode circuit, the dynamics of cascode switching will be discussed and the use of a Q_{RR} tester to evaluate the reverse-recovery characteristics of a cascode circuit will be explained. A comparison of the cascode's reverse recovery with that of a SiC MOSFET reveals that the JFET cascode actually performs better than the SiC MOSFET over temperature.

Further tests reveal that the cascode performs well at higher values of di/dt. Then, after presenting data on cascode robustness, some guidelines are given for selecting a low-voltage silicon MOSFET for use in JFET cascodes. Finally, a summary of the data presented here highlights the benefits of using a 1200-V SiC JFET in cascode versus a similarly rated SiC MOSFET, while also highlighting the JFET's dramatic improvement in performance versus a conventional IGBT.

1.0 Cascode Overview

A JFET and low-voltage MOSFET in a cascode configuration is shown in Fig. 1. The MOSFET is a normally off device, and the JFET is normally on. The JFET requires negative voltage to turn off.

From a steady-state perspective, the operation of the cascode circuit is straightforward: the JFET V_{GS} is the inverse of the MOSFET V_{DS}. Rephrased, the more positive the MOSFET V_{DS}, the more negative the JFET V_{GS}. This insures that when the MOSFET is off (V_{DS} increases), the JFET will turn off.

USCi's JFET threshold is typically centered at -6 V, so when the MOSFET is off, the MOSFET V_{DS} voltage will increase until it reaches the JFET's cutoff voltage.

When the MOSFET is on, the MOSFET V_{DS} and JFET V_{GS} are essentially zero, which insures the JFET is fully enhanced. USCi rates the R_{DS} of their JFETs at +2 V and 0 V VGS for cascode and direct-drive applications.

When the MOSFET's intrinsic diode conducts, the JFET is again fully enhanced, because the JFET's VGS will be one positive diode drop.

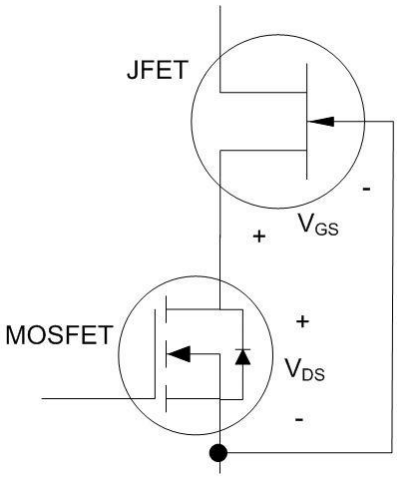

Figure 1: Cascode Configuration

2.0 Dynamics of Cascode Switching

The previous description of cascode operation is fine for steady state, but as most know, when changing states at high di/dt and dv/dt values, the results can differ from the ideal. The general concern during switching transitions is to insure there are not any inadvertent "excursions" that violate the device's absolute maximum ratings, generate excess losses or instability. A gate charge circuit is a good vehicle to analyze the dynamics of cascode circuits, since it easy to see the contribution of each parasitic element.

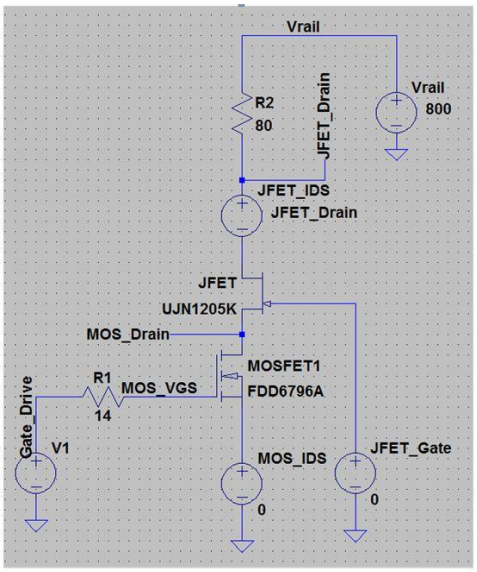

Figure 2: Cascode PSPICE Schematic

Using LTSPICE, a cascode circuit is implemented with USCi's UJN1205K and Fairchild's FDD6796A models (Fig. 2.) The MOSFET is driven with a 14-Ω gate resistor.

The cascode turn-on waveforms are shown in Fig. 3. The JFET V_{DS} (scaled down by 1/40 to fit scale such that 20 V is equivalent to 800 V) and the MOSFET VDS are the top waveforms (Fig. 3A.) The MOSFET VDS hovers above 7 V in the off state before the MOSFET's V_{GS} crosses threshold (Fig. 3D), and the MOSFET begins to turn on. The I_{GS} of the JFET flows as the MOSFET V_{DS} drops the JFET V_{GS} below threshold (Fig. 3C), and tails off as the JFET becomes fully enhanced.

The same waveforms are shown turning off in Fig. 4. The MOSFET turns off, but its V_{DS} does not immediately go back to 8 V, but increases to 19 V. This is due to the inductances between the JFET source and MOSFET drain (Fig. 4A.) This is critical, since the MOSFET V_{DS} is applied to the JFET V_{GS} and must not violate the absolute max. rating of

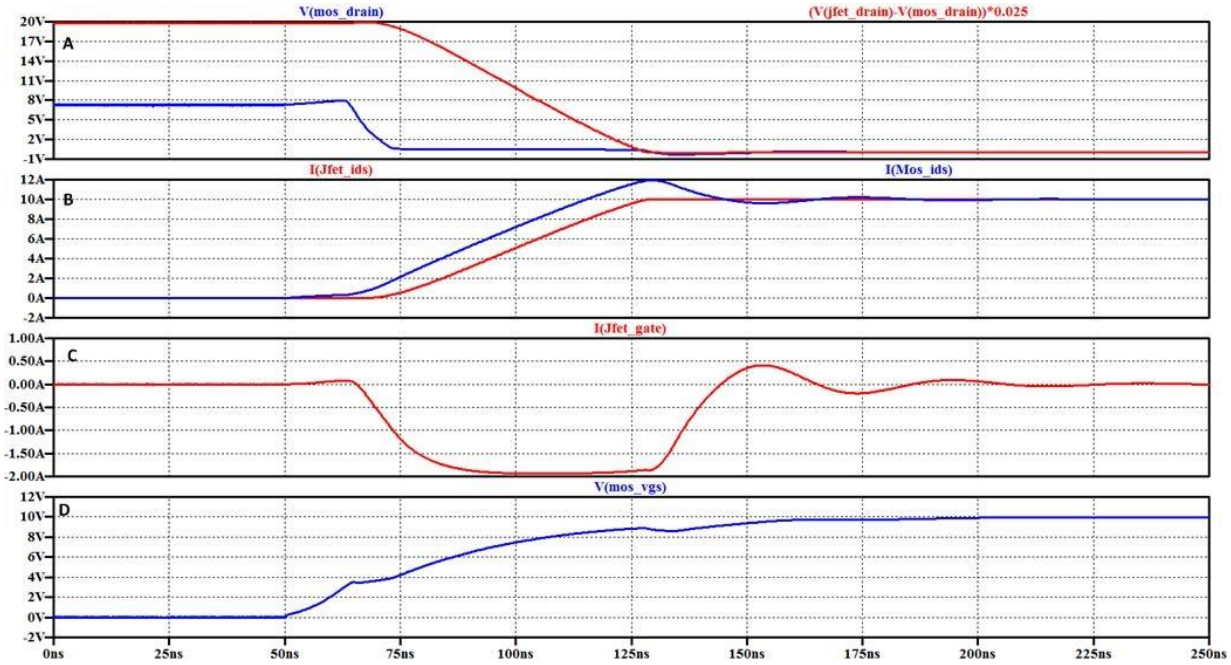

Figure 3: Cascode turn on

the JFET. The peak of the MOSFET VDS is due to the difference in turn-off time between the MOSFET and the JFET.

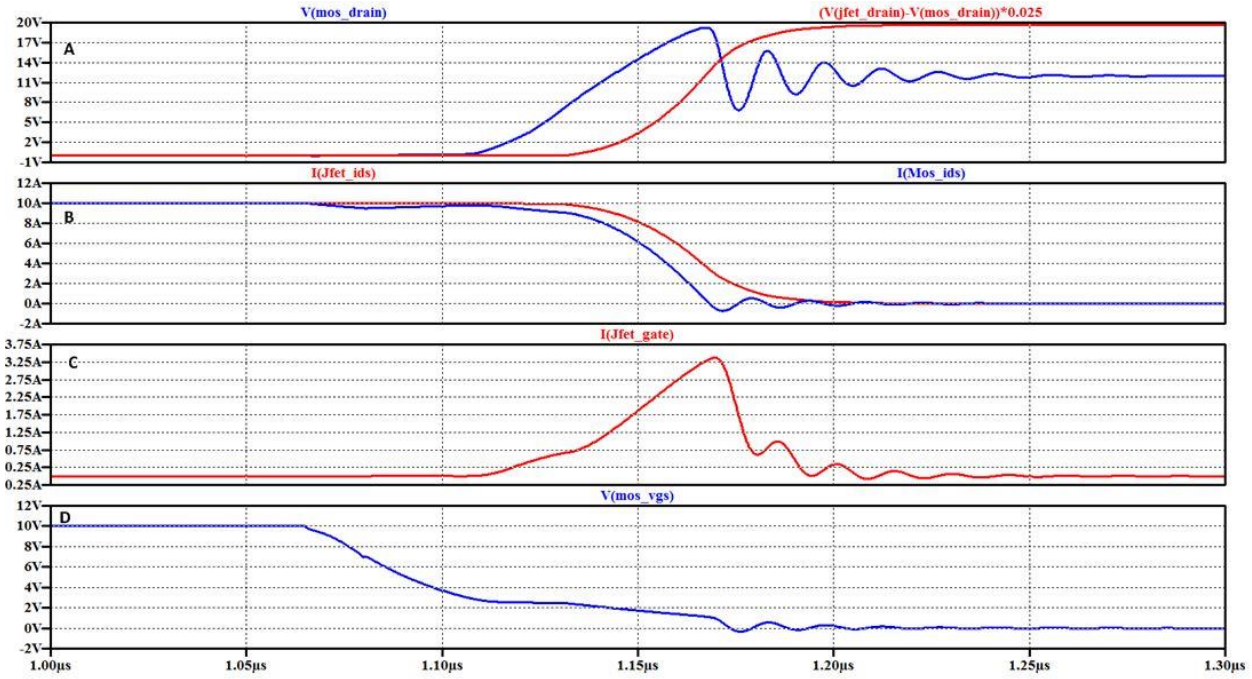

Figure 4: Cascode turn off

Ensuring that the JFET V_{GS} absolute maximum is not violated, and producing the ideal switching times for the application, there are several solutions. These solutions typically involve increasing the R_G for the MOSFET, and/or adding a zener (18 V)/resistor parallel combination from the JFET gate to MOSFET source.

3.0 Switching Inductive Loads

Utilizing the MOSFET's intrinsic diode in cascode to pass current was briefly described at the beginning of this note. This diode must also reverse bias and block voltage. A diode Q_{RR} tester is used to evaluate the reverse-recovery characteristics of a cascode. Fig. 5 is a schematic of a diode Q_{RR} tester with a cascode in the device under test position (D.U.T.)

A Q_{RR} tester applies two pulses. The first pulse turns the low-side device on, and the current ramps through the inductor. At the desired test current, the low side is turned off and the CT node goes positive until it is clamped by the MOSFET's intrinsic diode within the cascode.

There is very little reduction in current, since the voltage drop across the inductor is very small (MOSFET V_{SD} + JFET R_{DS}*I_F).

The low-side device is turned back on and CT is pulled back to ground. During this transition, the MOSFET's intrinsic diode must reverse bias and block voltage.

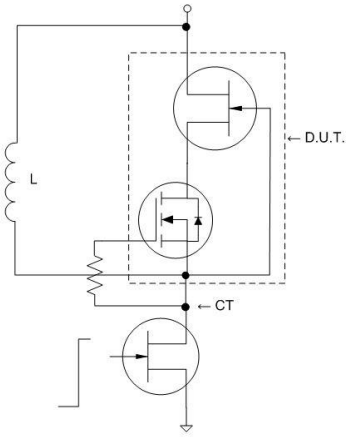

Figure 5: Q_{RR} Test Circuit

The charge lost during this reverse bias is a loss component, and depending on the amount of charge or the switching frequency can be significant with respect to the overall system efficiency.

A Q_{RR} test fixture is configured with the D.U.T being a UJN1205K, 45-mΩ 1.2-kV JFET plus an AO472A, 5-mΩ, 30-V MOSFET cascode with a 3-Ω gate resistor between the MOSFET gate and source to simulate a driver impedance. The low-side gate-drive timing delivers a test current at 19 A with a di/dt of 0.25 A/ns from an 800-V rail.
The measurements are taken at 25°C and 125°C. There are three graphs in Fig. 6 due to test equipment limitations. The cascode JFET and MOSFET are heated individually per test.

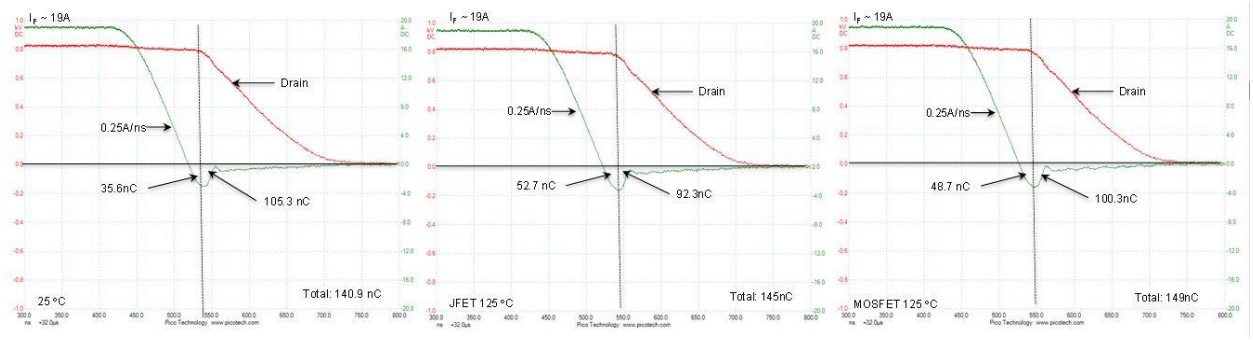

Figure 6: Cascode Reverse Recovery

Moving left to right across Fig. 6, the 25°C Q_{RR} is 140.9 nC, and the JFET and MOSFET 125°C values are 145 nC and 146 nC respectively. Extrapolating from this data, a SiC JFET cascode will have an increase of no more than 10% in Q_{RR} charge over a 100°C rise. In this example, using the 125°C results, the energy loss attributed to Q_{RR} would be 70 µJ per cycle, which at 100 kHz translates to a loss of 7 W.

How does this compare to other silicon carbide technologies? The same test conditions were applied to an 80-mΩ SiC MOSFET using its intrinsic diode for reverse recovery.

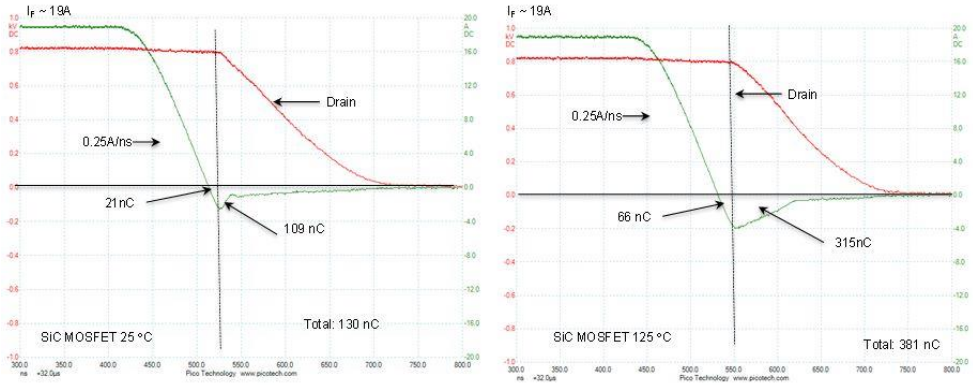

Figure 7: SiC MOSFET Reverse Recovery

The results are shown in Fig. 7. At 25°C the Q_{RR} is 130 nC, which is a good number, and expected given that the device is twice the R_{DS} of the JFET in the previous cascode tests.

At 125°C the SiC MOSFET reverse recovery almost triples, going to 381 nC of charge. Translating the loss at this temperature would be 144 µJ per cycle or 14.4 W at 100 kHz.

This comparison illustrates that a JFET cascode configuration can successfully use the MOSFET's intrinsic diode and compete against other device structures that have their own intrinsic diode.

3.0 di/dt Comparison

The previous cascode tests were done at 0.25 A/ns. In this comparison, a USCi 80-mΩ JFET (UJN1208K) will be compared at 0.5 A/ns against the 45-mΩ JFET (UJN1205k) from the previous measurements.

The cascode MOSFET will be the FDMC8296, an 8-mΩ 30-V device in 3 x 3 MLP packaging.

The 3 x 3 MLP may not be ideal for all power levels, but it has good thermal performance for its size and lower inductance than the DPAK, so it matches well with the USCI's 80-mΩ JFET and higher values of di/dt.

The results are shown in Fig. 8, and the Q_{RR} values come in close to the proportion of the R_{DS} ratio. With a 15-A test current and twice the di/dt of the previous cascode measurements the Q_{RR} of the 80-mΩ JFET measures 58 nC, while the 45-mΩ JFET comes in at 93 nC. This performance bodes well for applications requiring higher values of di/dt.

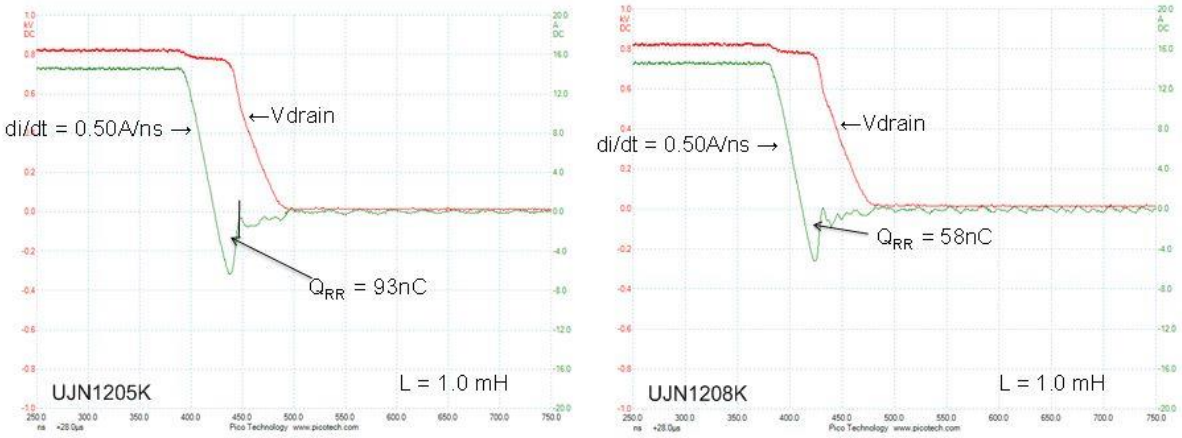

Figure 8: 45 mΩ to 80mΩ JFET Reverse Recovery Comparison

4.0 Robustness of Cascode

Two key indicators for robustness are short circuit and avalanche capability. The high-temperature capability of SiC is well documented, but how does it perform in cascode? In Fig. 9, a cascode made up of the 45-mΩ, 1.2-kV JFET

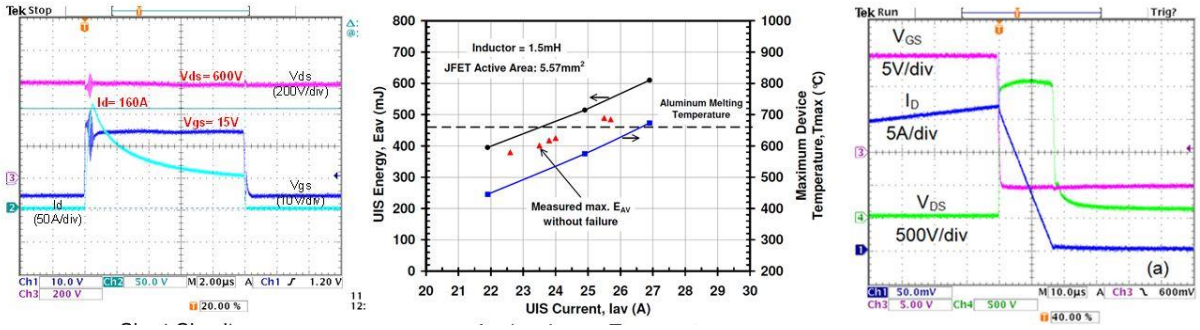

Figure 9: SiC MOSFET Reverse Recovery

(UJN1205k) and the AOD472A MOSFET is subjected to a series of tests. On the far left, the cascode is connected across a 600-V source and pulsed for 10 µs. The current spikes to 160 A with minimal deflection in the 600-V rail, and the cascode remains in control at all times.

With respect to avalanche capability, the same cascode configuration is subjected to a series of avalanche tests until failure (middle chart). The results of these tests indicate that failures occurred when the aluminum melting point was reached and the top metal is vaporized off the die.

The single avalanche waveform on the right is an avalanche energy of 392 mJ energy with the device avalanching at 2000 V. These results indicated that there is plenty of "head room" when operating these devices within their ratings.

6.0 Choosing a MOSFET for a Cascode

Since the MOSFET will have significant influence on the dynamics of the cascode circuit, it is important to select the correct device. It is not a case of "one size fits all."

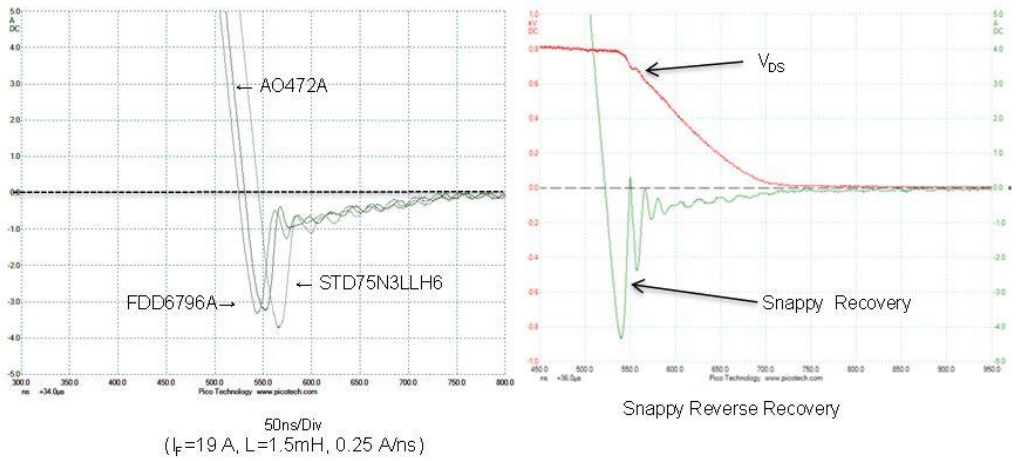

Figure 10: Comparison of Cascode Reverse Recovery for different MOSFETs

MOSFET data sheets traditionally have about three specifications for intrinsic diode performance (t_{RR}, Q_{RR} and V_{SD}). It is rare that these values are generated at the end user's di/dt. Even if softness (S) is included in the data sheet, there is no way to know if there are abrupt di/dt's with the recovery, or excessive ringing.

In Fig. 10 there is a comparison of some of the MOSFETs evaluated for cascode performance. The devices were chosen from their datasheet values and then compared on a QRR tester. The waveforms on the left are ones that were deemed acceptable, and the one on the right was discounted due to excessive IRM and ringing.

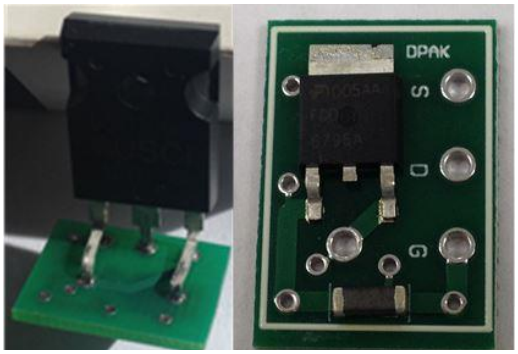

Figure 11: Cascode Test Board

The selection of the devices followed a simple protocol. Since RDS and QRR are inversely proportional, a good rule of thumb is to keep the RDS in the 10% range of total series resistance (JFET RDS(ON) + MOSFET RDS(ON).) Once the RDS(ON) value was established, a number of devices from manufacturers were sorted and selected for their minimum QRR value. These devices were mounted on small cascode test boards and evaluated on a QRR tester. Three out of four devices were found acceptable.

If a designer does not have access to a Q_{RR} tester, he or she can consult a list of recommended MOSFETs maintained by USCi. And time permitting; USCi is even willing to test specific devices for customers. The USCi application team has customer test boards available for Q_{RR} or in-circuit system evaluations (Fig. 11.)

7.0 Summary

A summary of the previous waveforms and some additional data on IGBTs are shown in Tables 1 and 2. Since manufacturers do not use the same current-rating methodology, a calculated conduction loss for 20 A at 100% duty cycle has been added to the chart as reference for the overall device capability. The 5 mΩ for the cascode MOSFET has been included in the conduction loss (AOD472A.)

		25°C						
Device	di/dt	P_C (20 A)	$I_{RM(pk)}$	t_a	t_b	t_{rr}	Q_{RR}	S
	A/ns	W	A	ns	ns	ns	nC	
JFET Cascode (1.2 kV, 45 mΩ + 5 mΩ)	0.25	20	3.0	18.6	17.4	36	141	0.94
SiC MOSFET (1.2 kV,98 mΩ)	0.25	39	2.5	13.6	12.8	26.4	130	0.94
IGBT Co-pak (1.2 kV, 30 A/25°C)	0.25	41	5.0	22.8	28.2	51	504	1.24

Table 1. Comparing reverse recovery of SiC JFET + silicon MOSFET cascode versus SiC MOSFET and IGBT at room temperature.

		125°C							
Device	di/dt	P_C (20 A)	$I_{RM(pk)}$	t_a	t_b	t_{rr}	Q_{RR}	S	E(125°C)
	A/ns	W	A	ns	ns	ns	nC		µJ
JFET Cascode (1.2 kV, 45 mΩ + 5 mΩ)	0.25	36	3.2	22.2	13	35.2	153.1	0.59	70
SiC MOSFET (1.2 kV,98 mΩ)	0.25	68	4.0	19.4	86	105.4	381	4.43	370
IGBT Co-pak (1.2 kV, 30 A/25°C)	0.25	50	8.0	34.8	102	136.8	863	2.93	144

Table 2. Comparing reverse recovery of SiC JFET + silicon MOSFET cascode versus SiC MOSFET and IGBT at high temperature.

When analyzing the cascode against competing technologies, the most apparent difference is how stable the SiC JFET/SiC MOSFET comparison is over temperature, and how the addition of the MOSFET enhances the overall performance of the circuit. Not only does the cascode allow operation with a standard gate drive (V_{GS}: 0 V to 10 V), the intrinsic diode delivers the lowest QRR at temperature. The cascode's QRR increases only 10% over a Tj rise of 100°C (the sum of 125□C MOSFET and JFET data.) The IGBT co-package values are given for reference for evaluating the use of a new technology.

It is clear that a designer can implement a cascode configuration, and with careful selection of the components not have to make performance compromises, but can actually improve performance over a single-device solution. Since there are many different applications and operating points, this note cannot cover all events that may come up when optimizing for performance.